Assignment Report

Name : Ansh J. Kanadiya

Batch : C04B

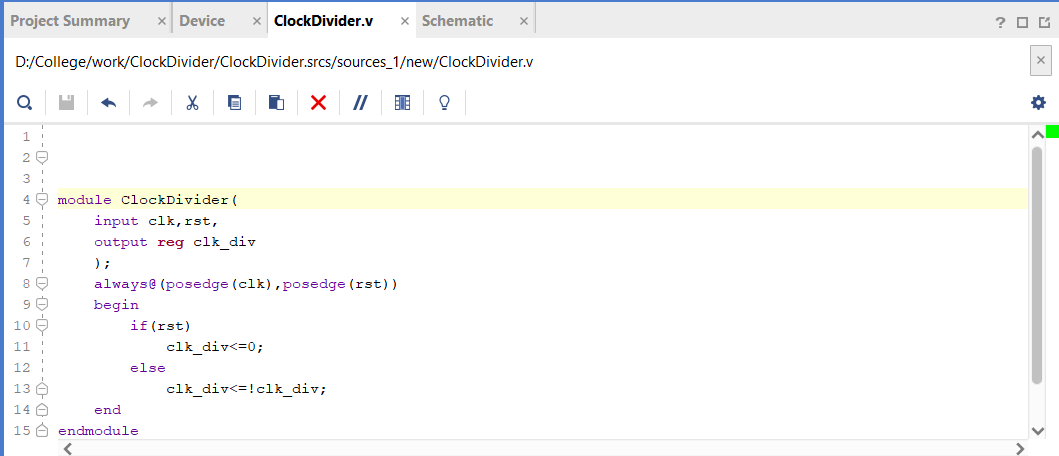
Branch : Electronics (EL)

I.D. No. : 21EL005

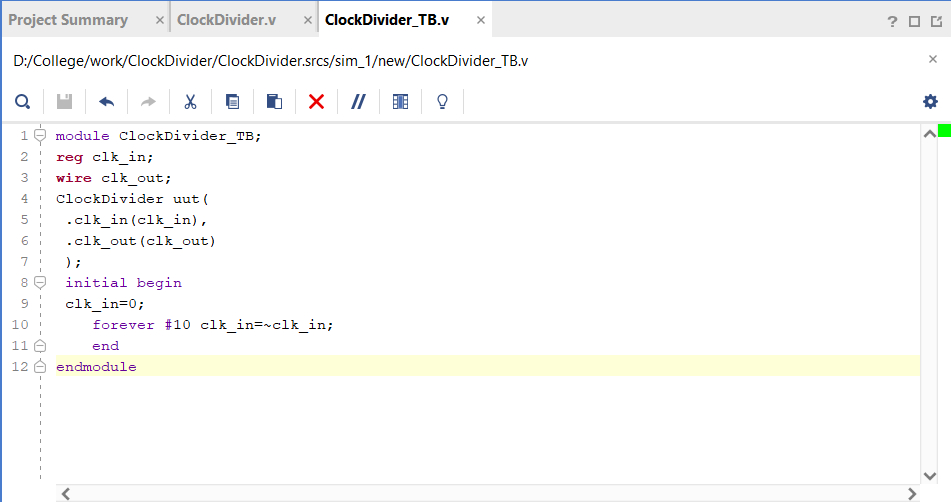
College : Birla Vishwakarma Mahavidyalaya

1. **Clock Divider :-**

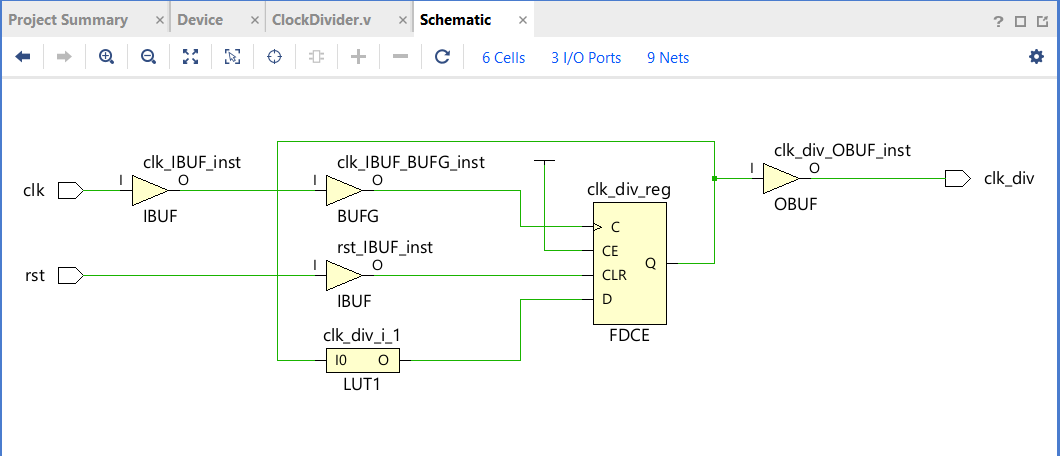
Verilog Code:



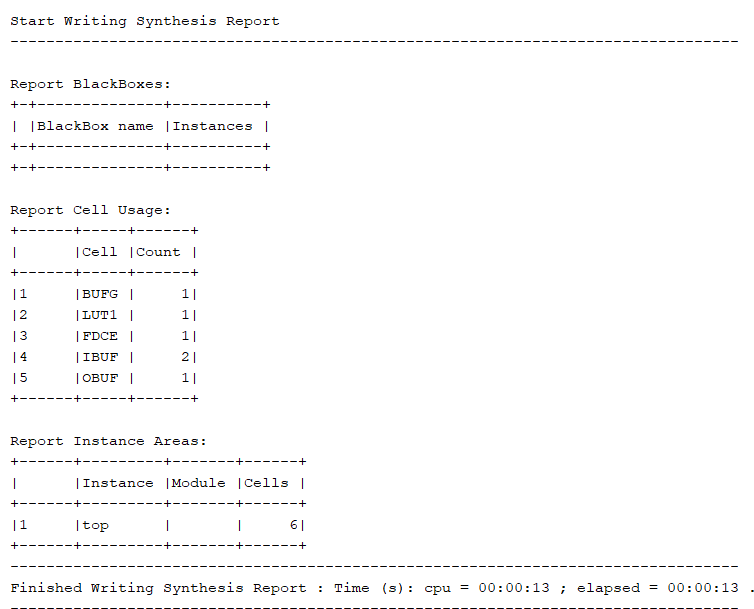
Test Bench:



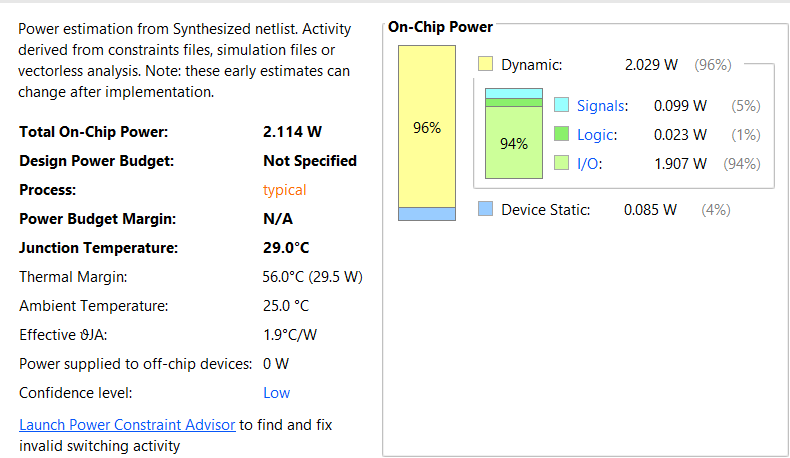
RTL Schematic:



Synthesis Report:

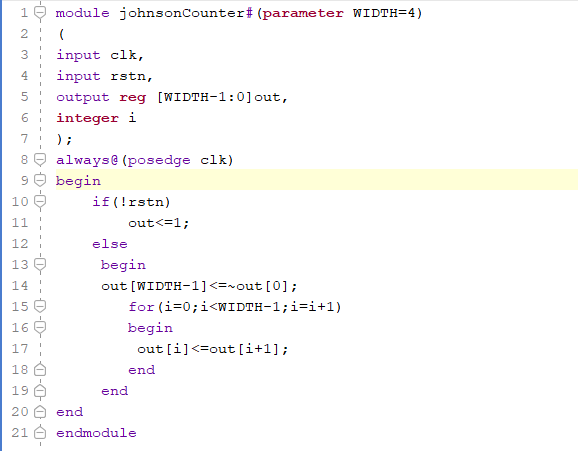


Power Report:

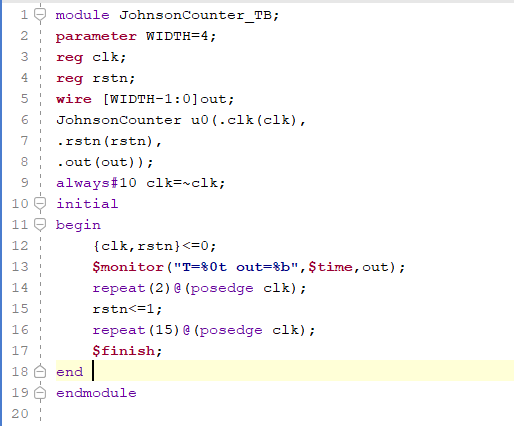


1. **Johnson Counter :-**

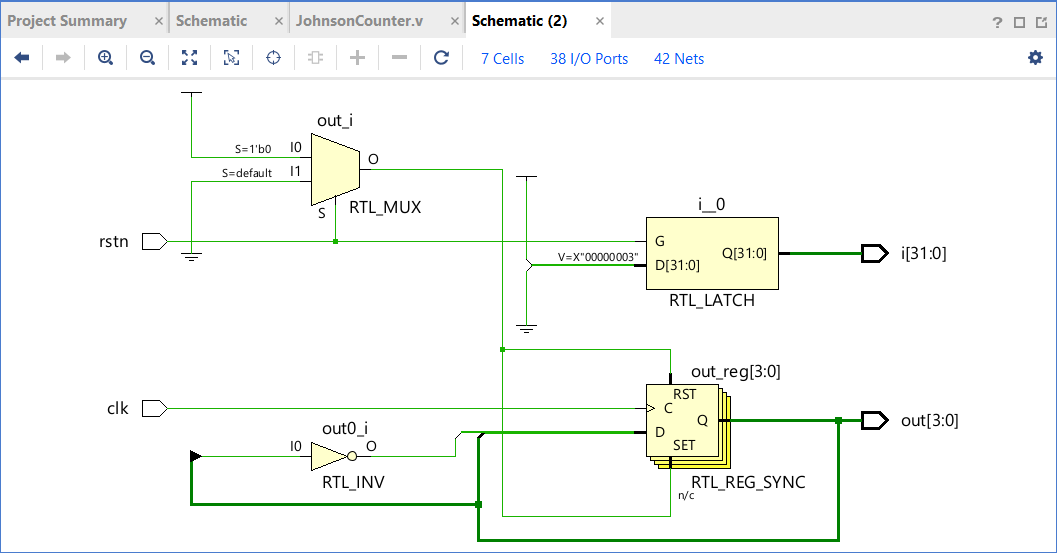
Verilog Code:



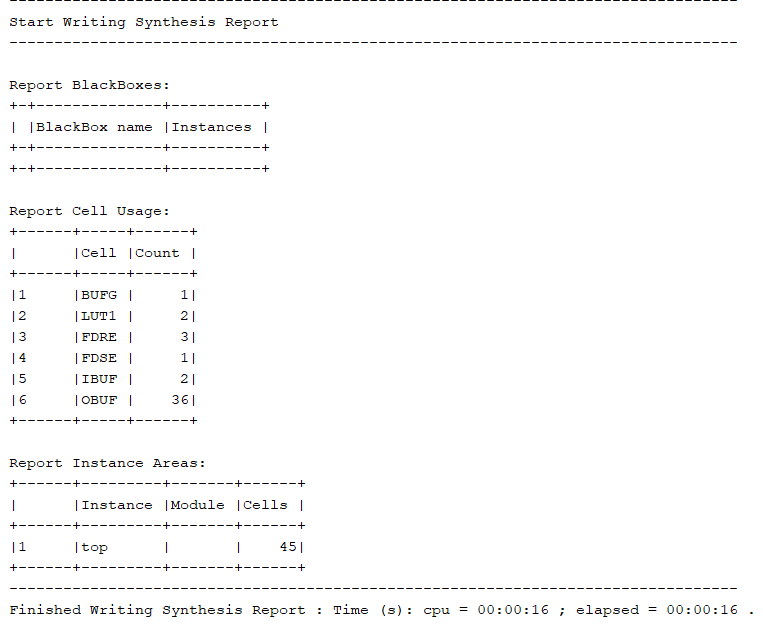
Test Bench:



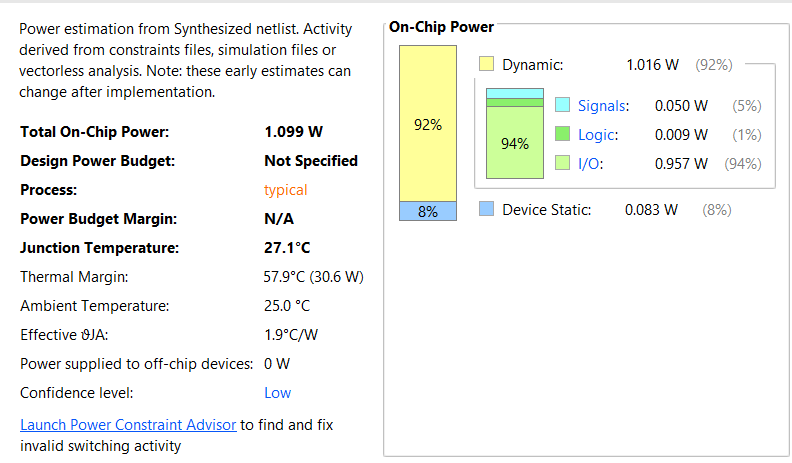
RTL Schematic:



Synthesis Report:

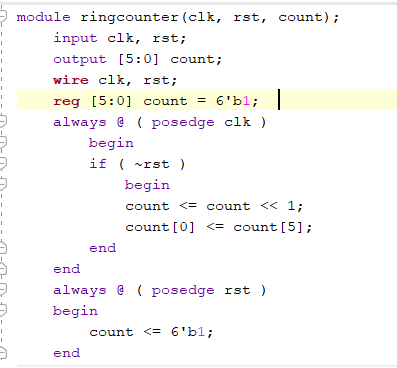


Power Report:

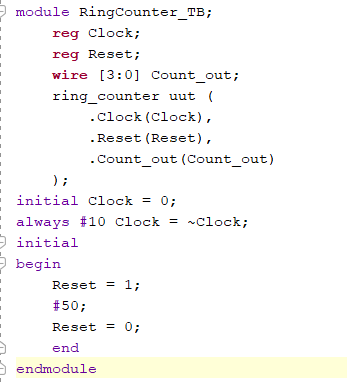


1. **Ring Counter :-**

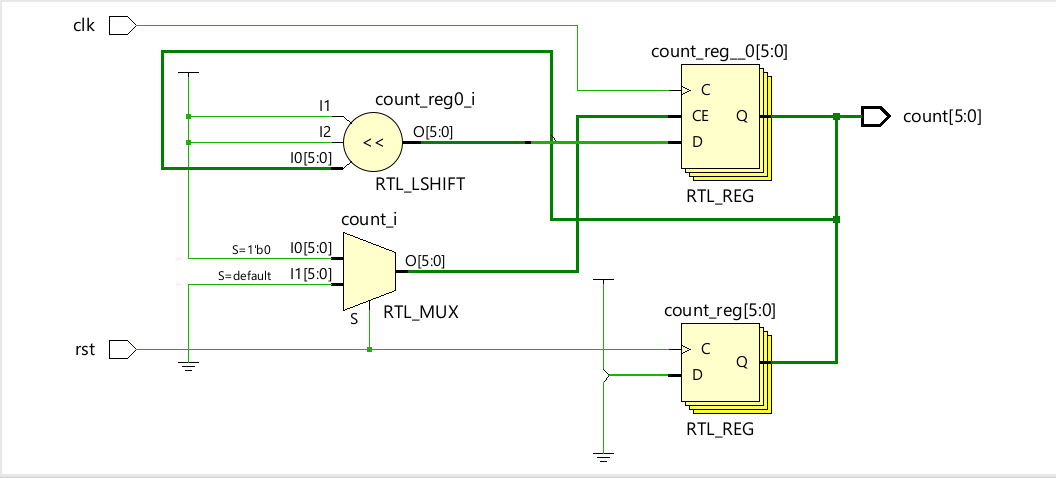
Verilog Code:



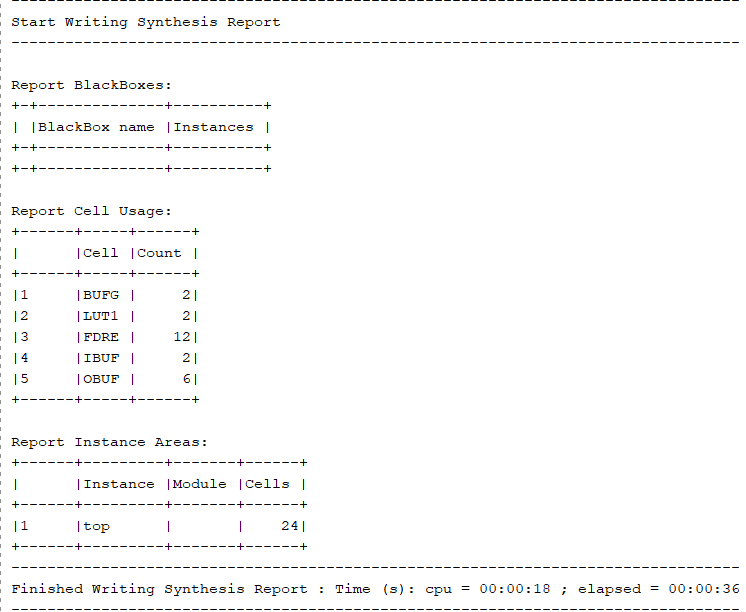
Test Bench:



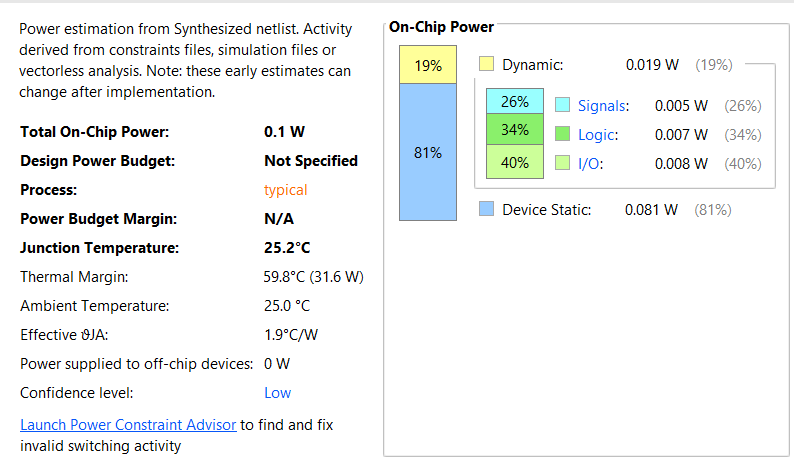
RTL Schematic:



Synthesis Report:

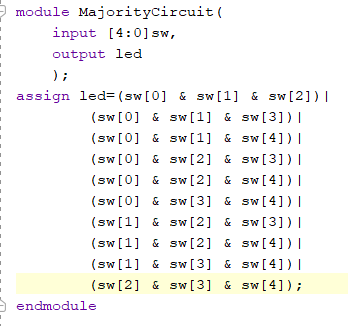


Power Report:

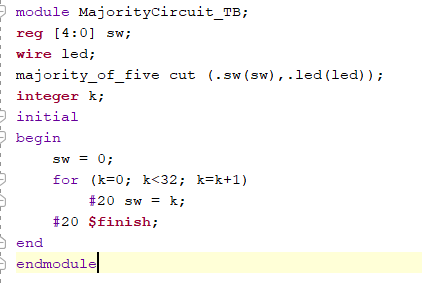


1. **5 Input Majority Circuit :-**

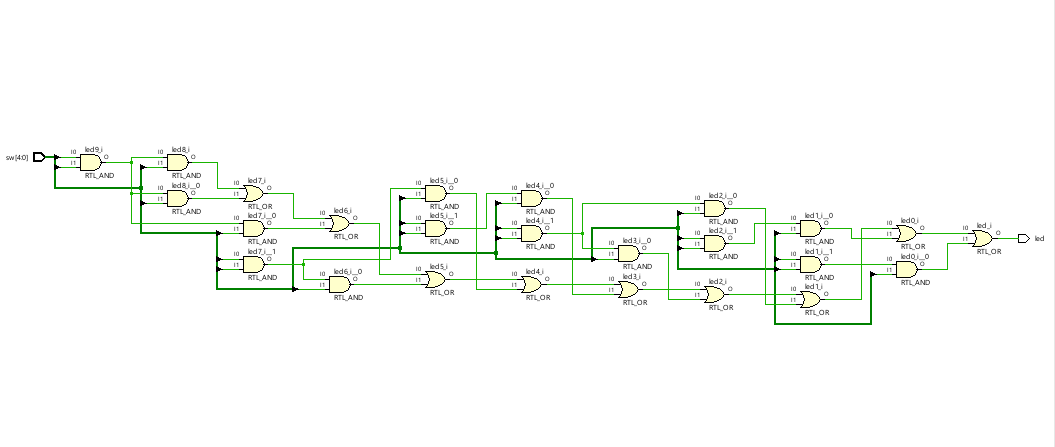
Verilog Code:



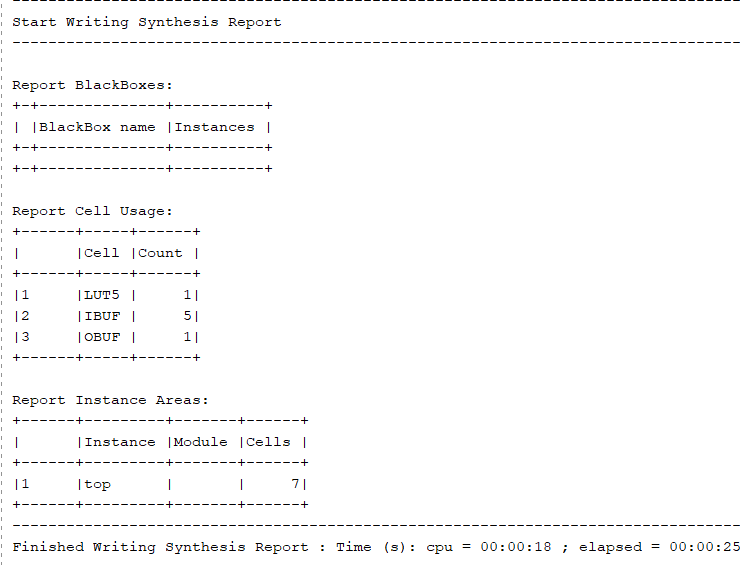
Test Bench:



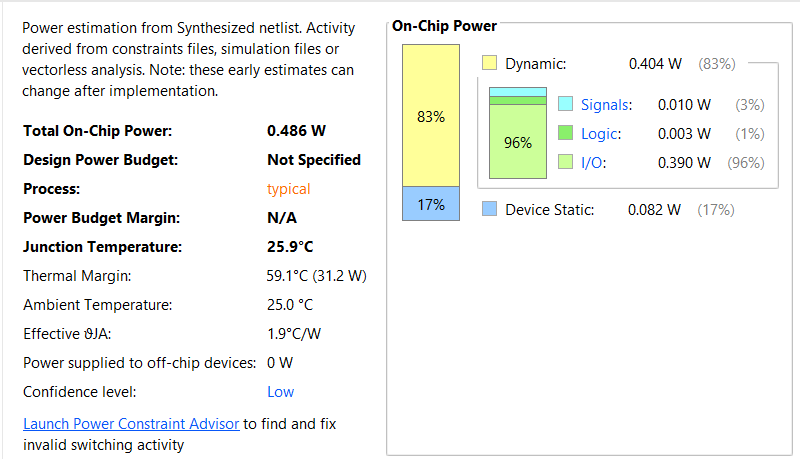
RTL Schematic:



Synthesis Report:

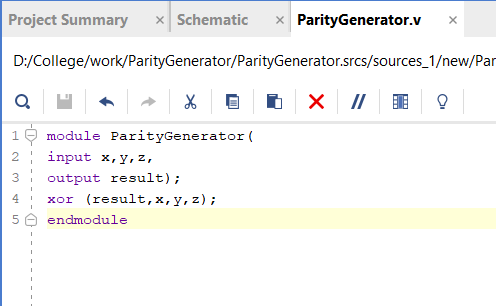


Power Report:

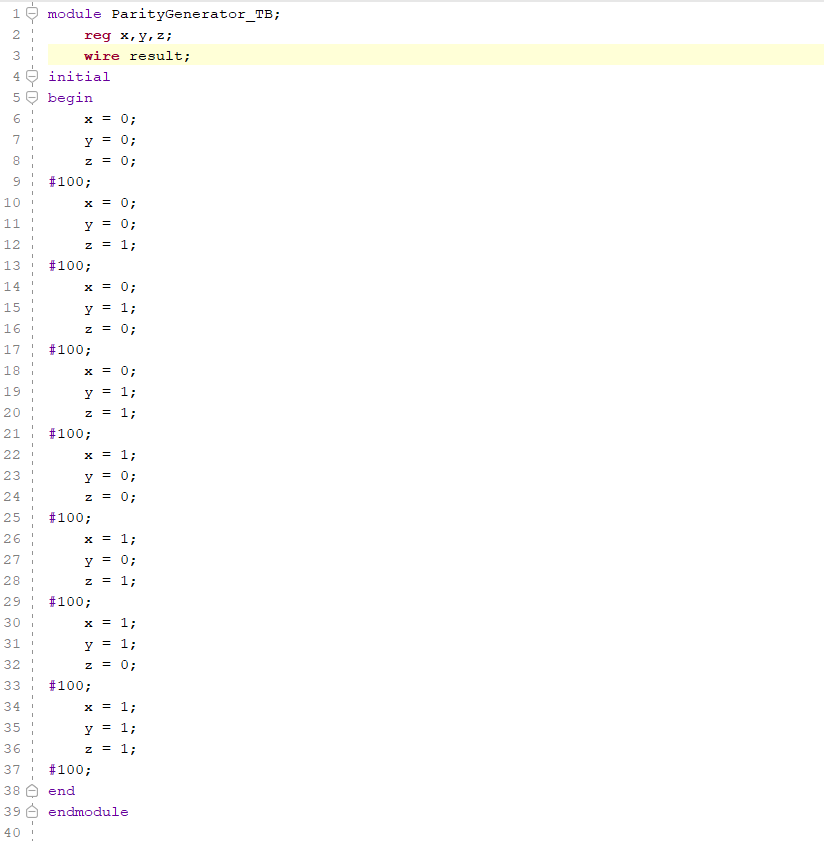


1. **Parity Generator :-**

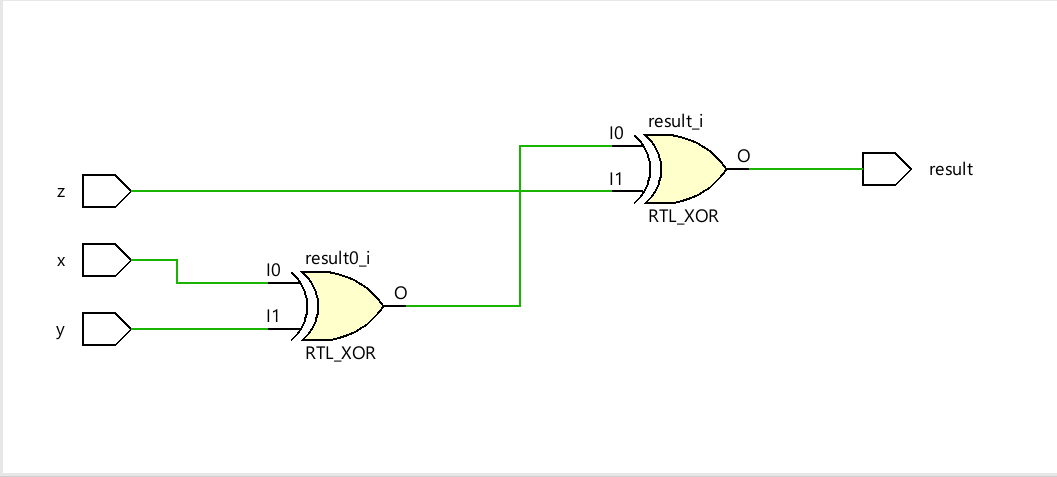
Verilog Code:



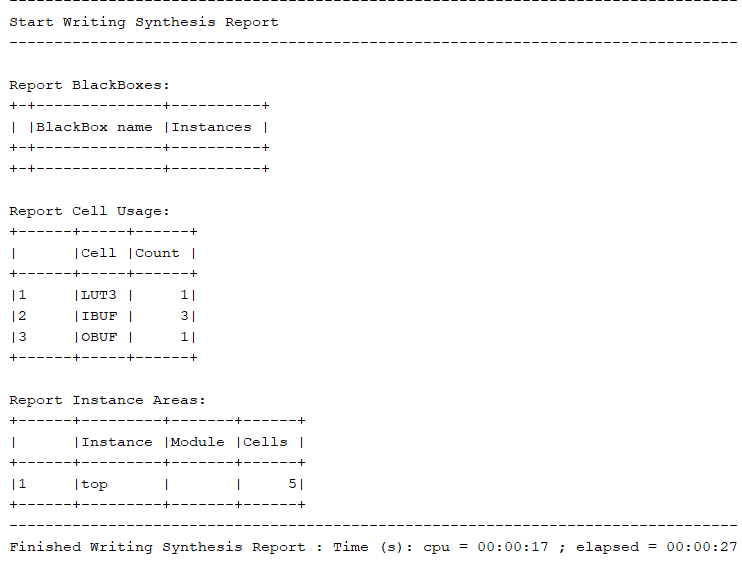
Test Bench:



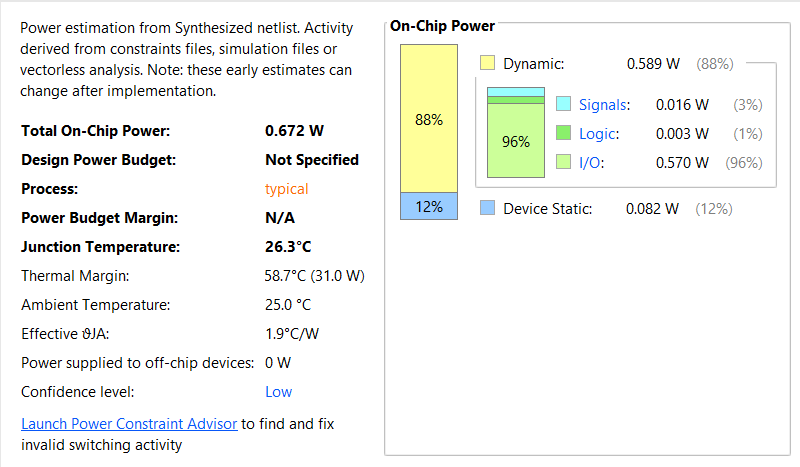
RTL Schematic:



Synthesis Report:

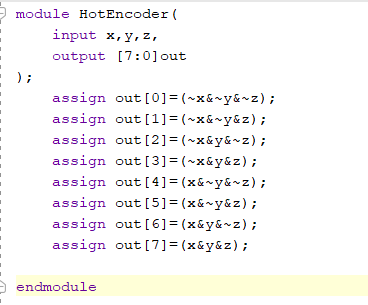


Power Report:

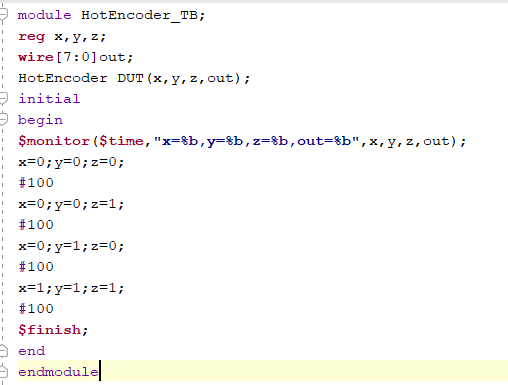


1. **Binary To One Hot Encoder :-**

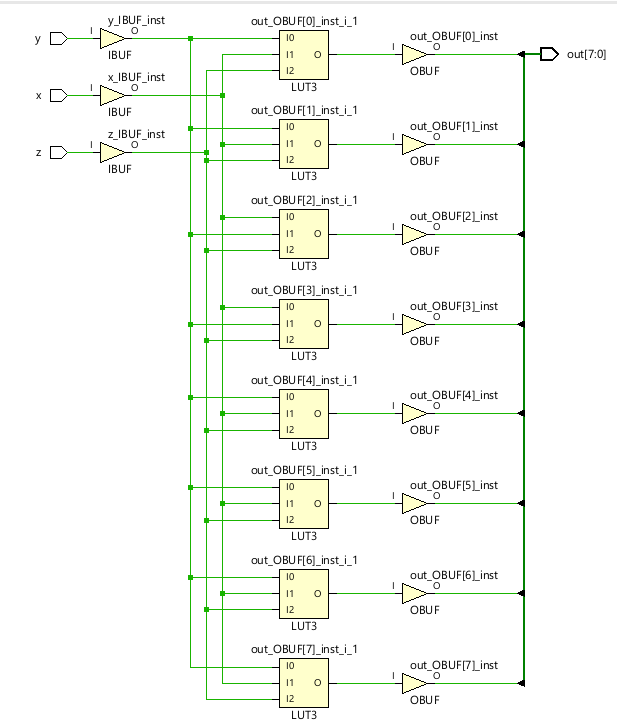
Verilog Code:



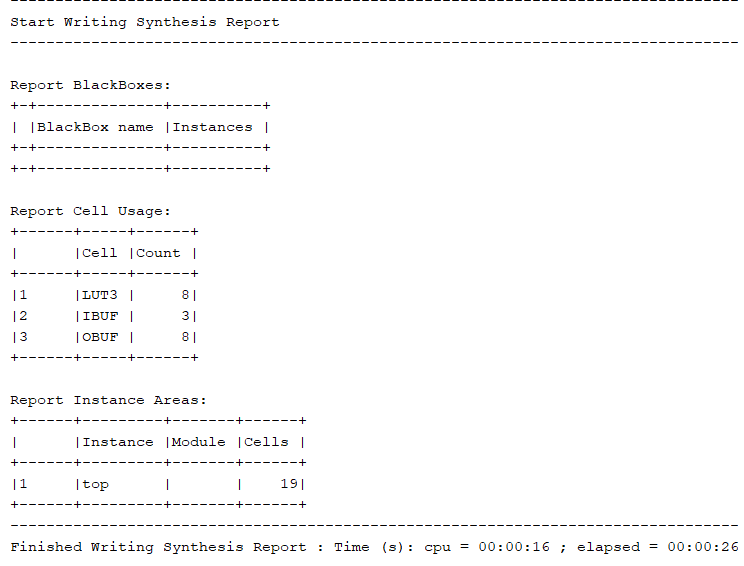
Test Bench:



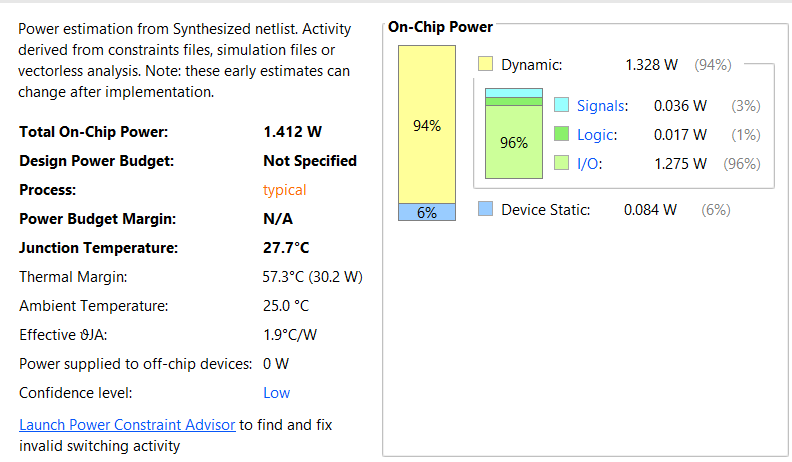
RTL Schematic:



Synthesis Report:

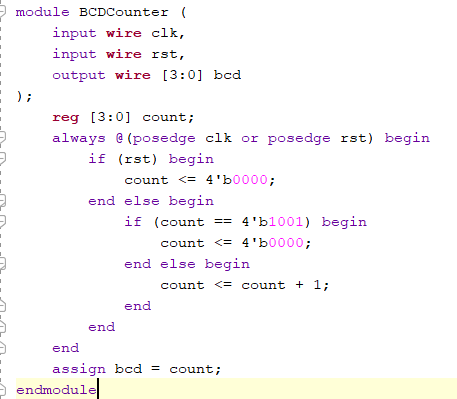


Power Report:

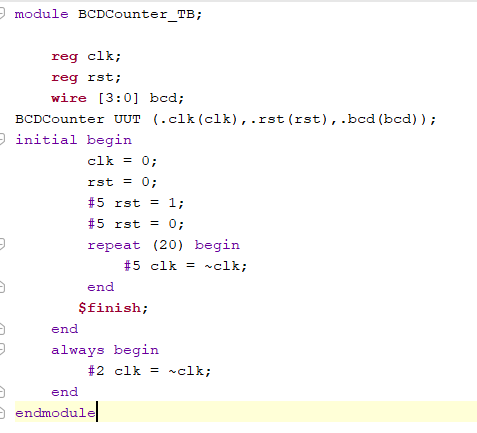


1. **4 Bit BCD Synchronous Counter :-**

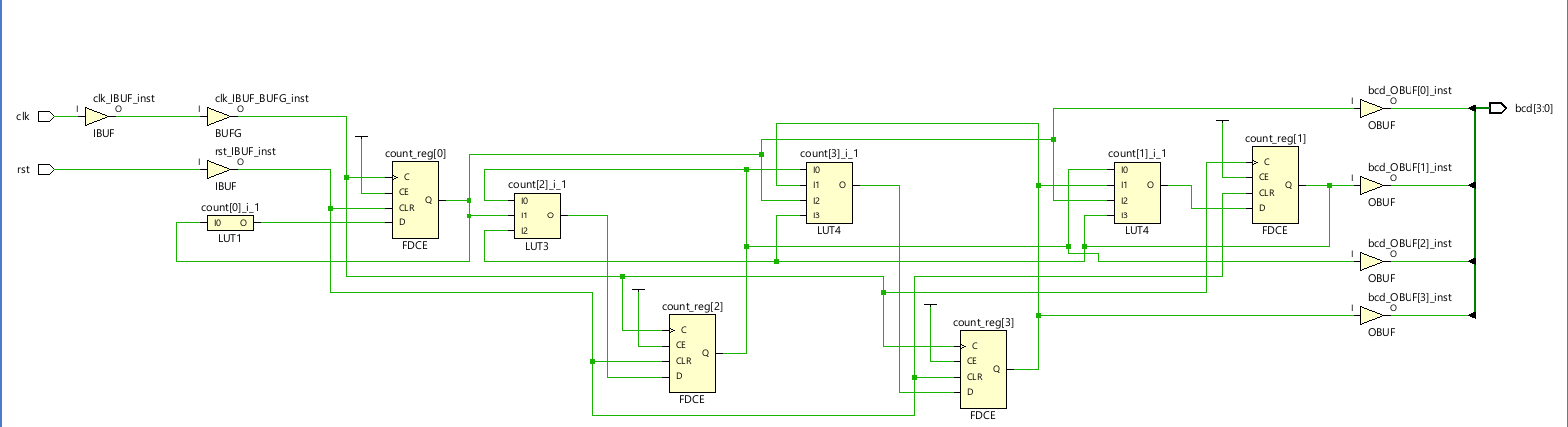
Verilog Code:



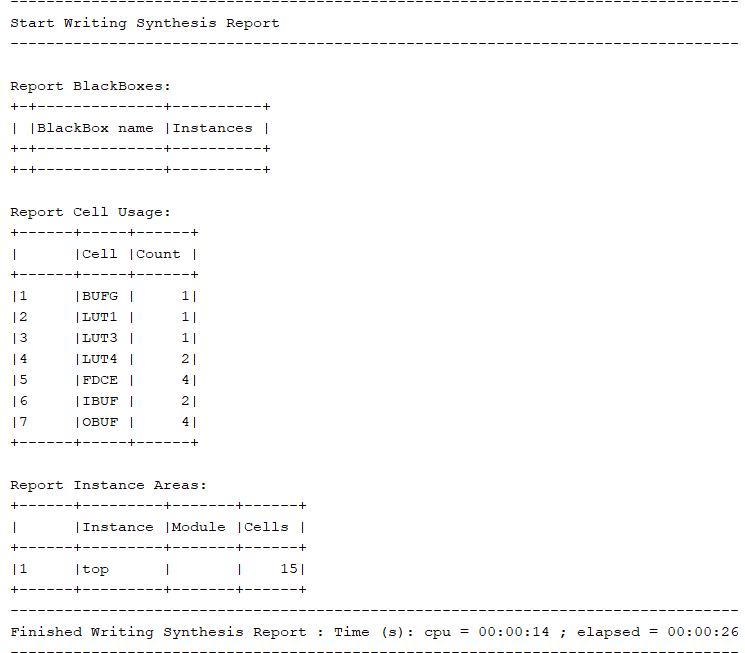
Test Bench:



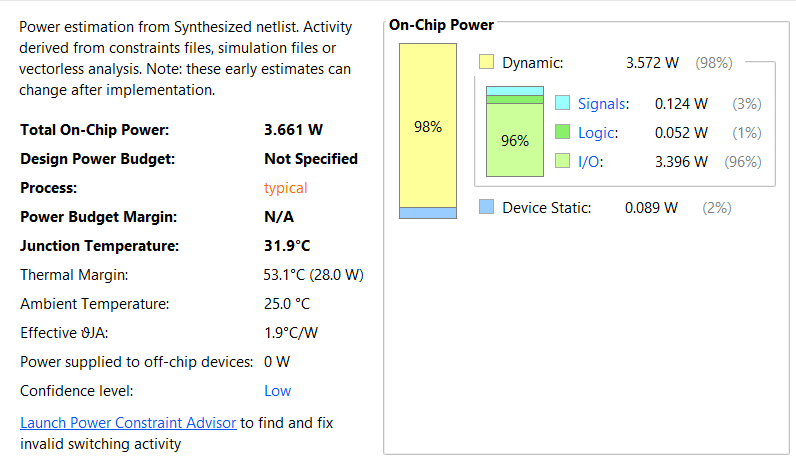
RTL Schematic:



Synthesis Report:

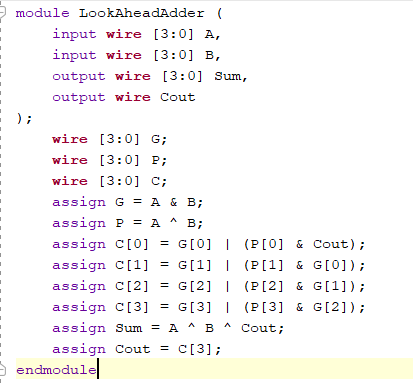


Power Report:

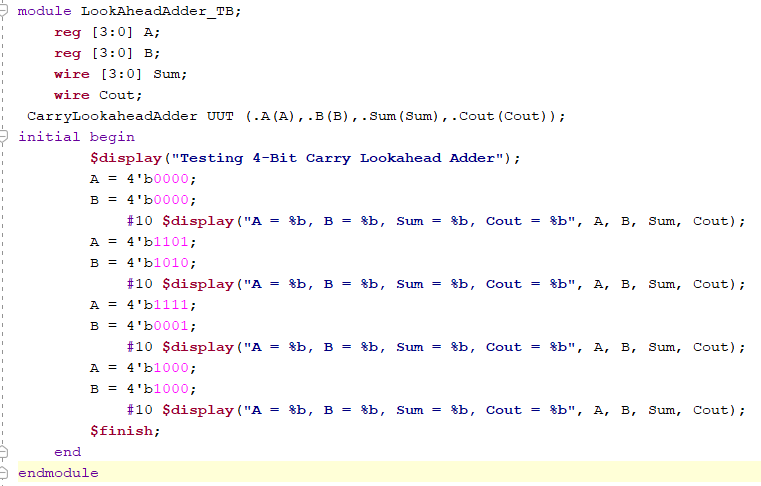


1. **4-Bit Carry Look Ahead Adder :-**

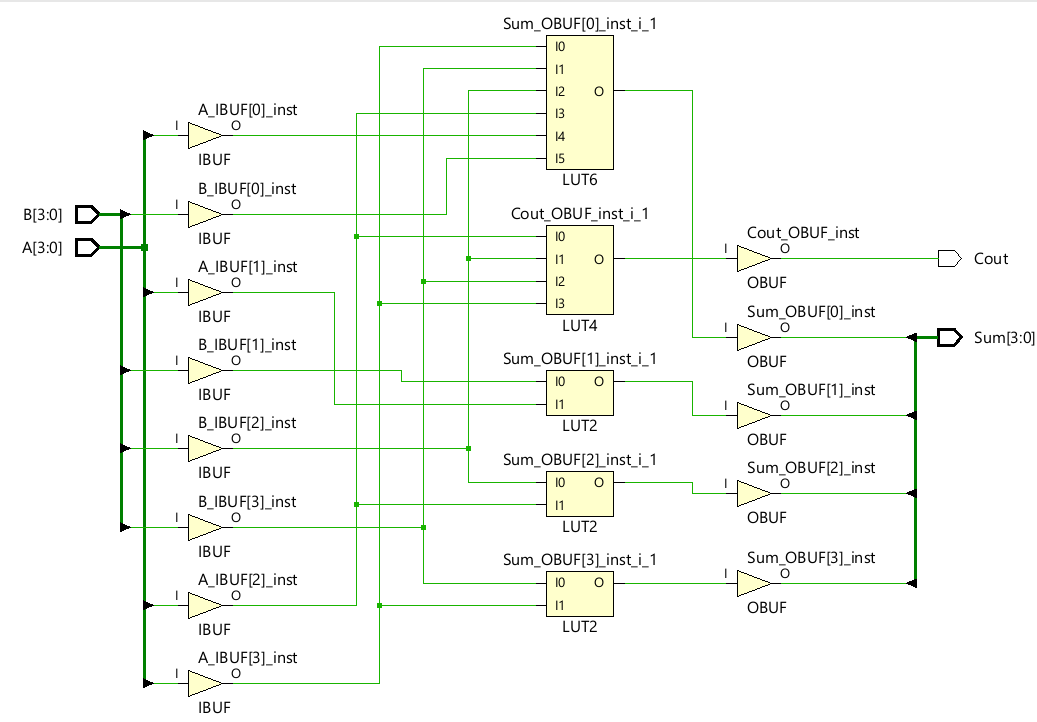
Verilog Code:

****

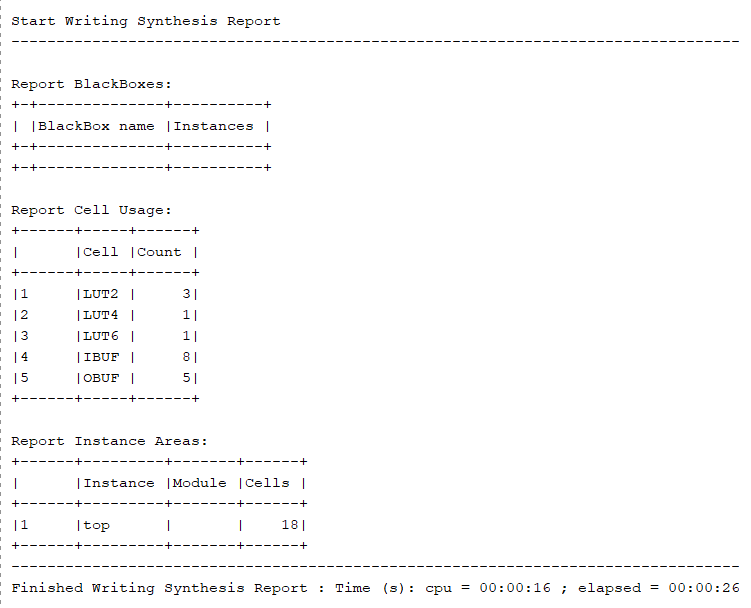
Test Bench:



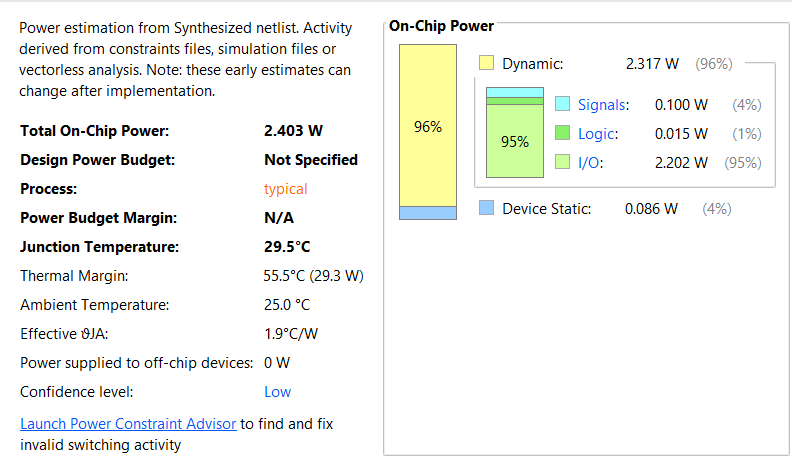
RTL Schematic:



Synthesis Report:

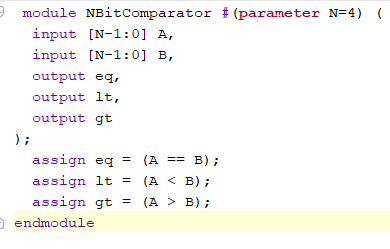


Power Report:

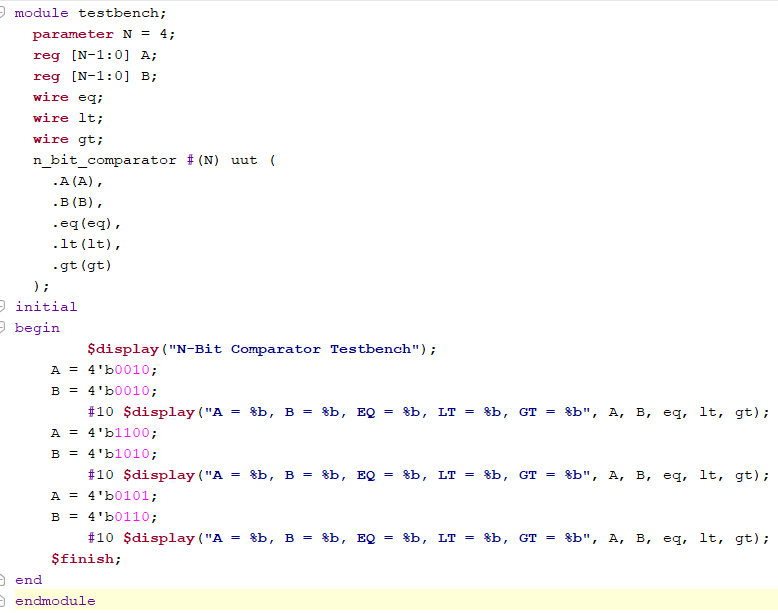


1. **N-Bit Comparator :-**

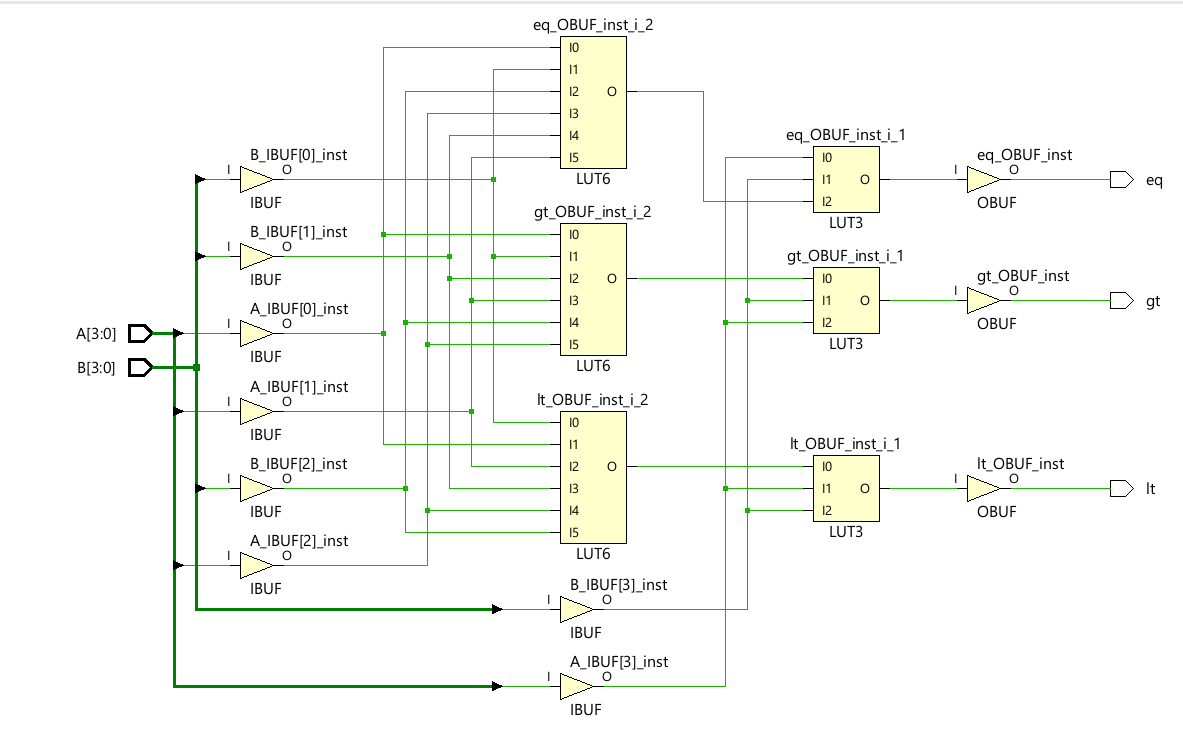
Verilog Code:

****

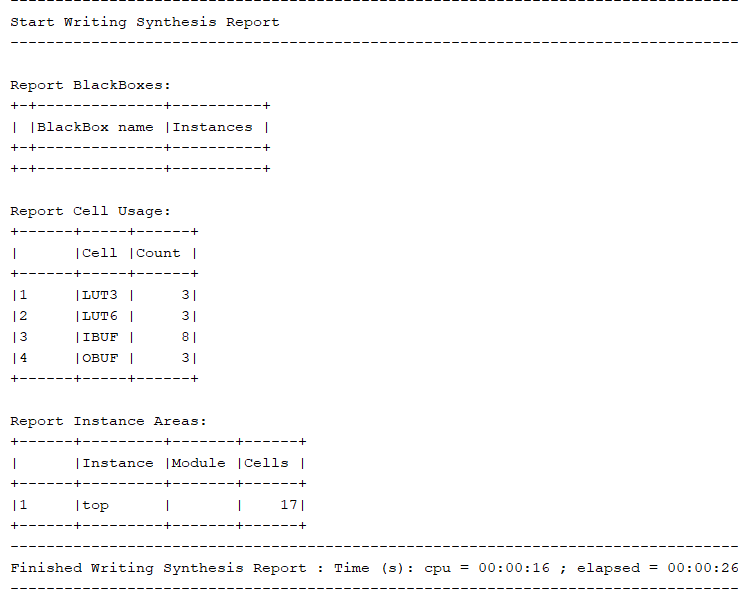
Test Bench:



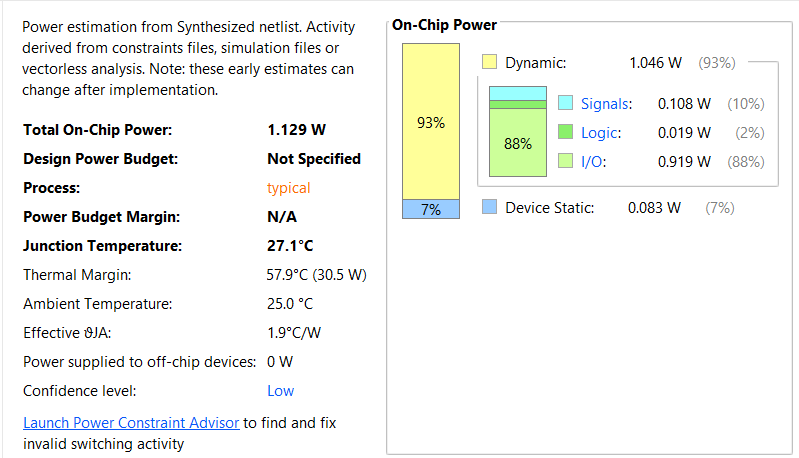
RTL Schematic:



Synthesis Report:

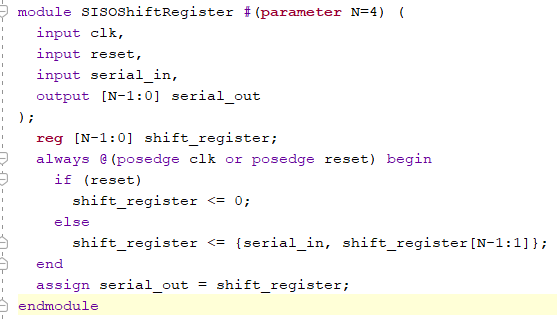


Power Report:

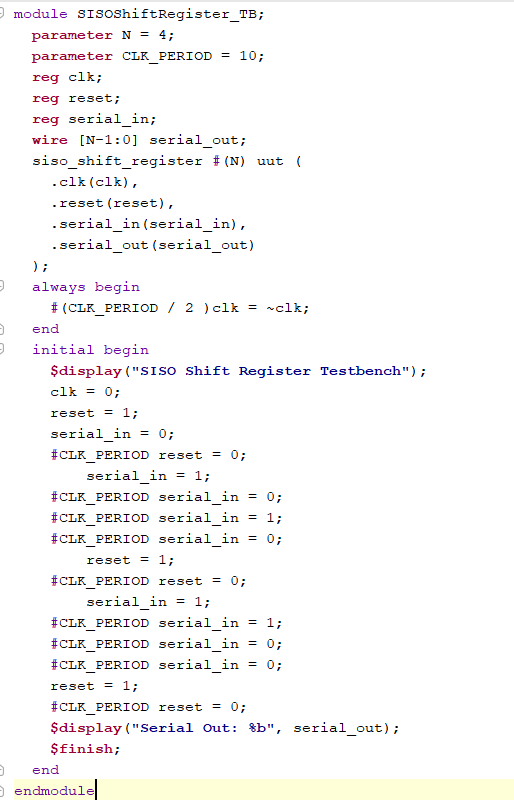


1. **Serial In Serial Out Shift Register :-**

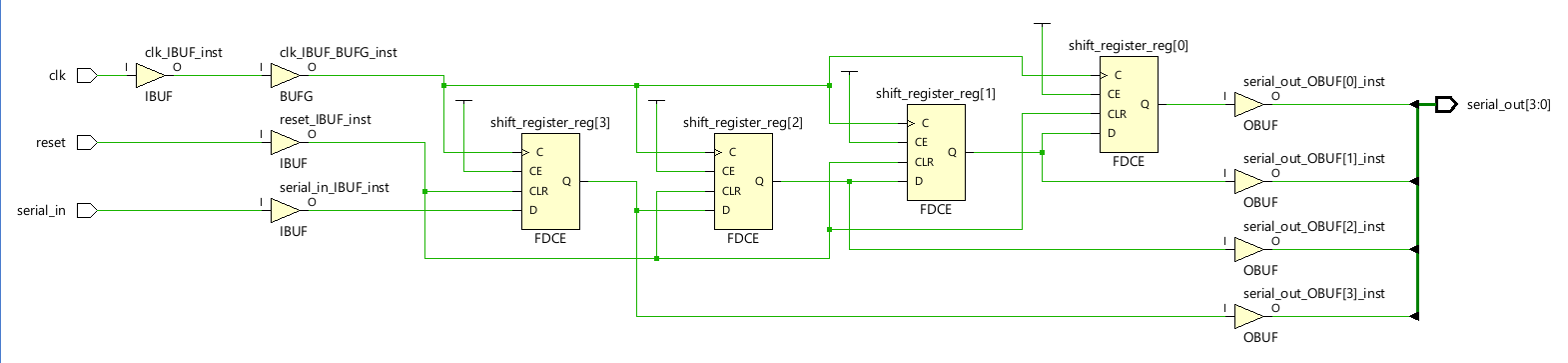
Verilog Code:



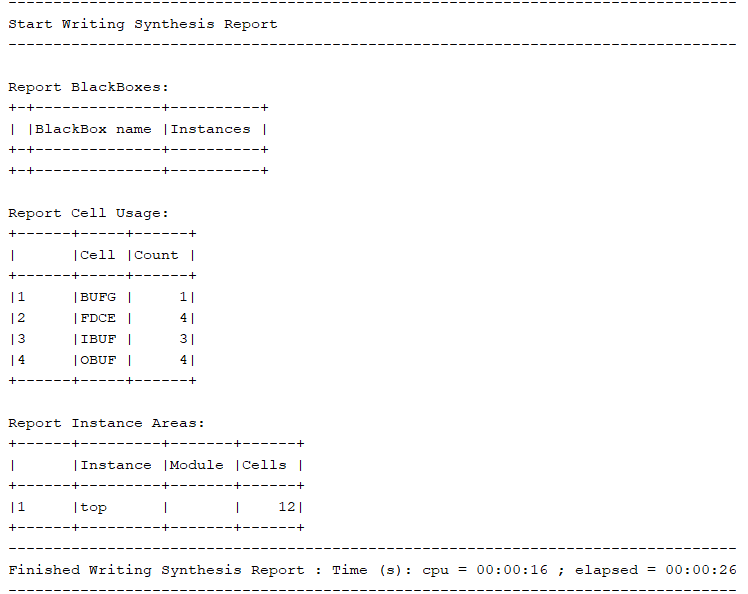
Test Bench:



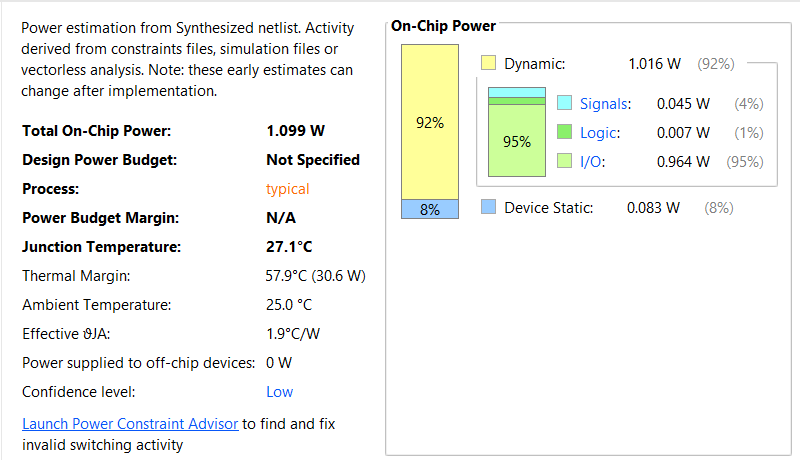
RTL Schematic:



Synthesis Report:

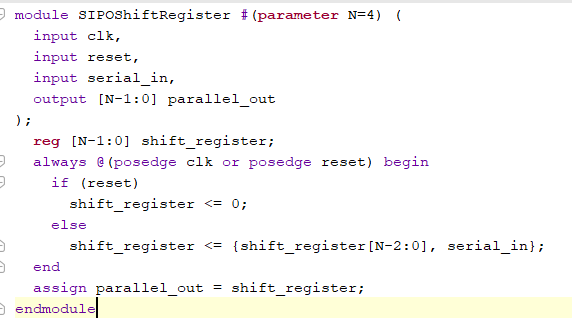


Power Report:

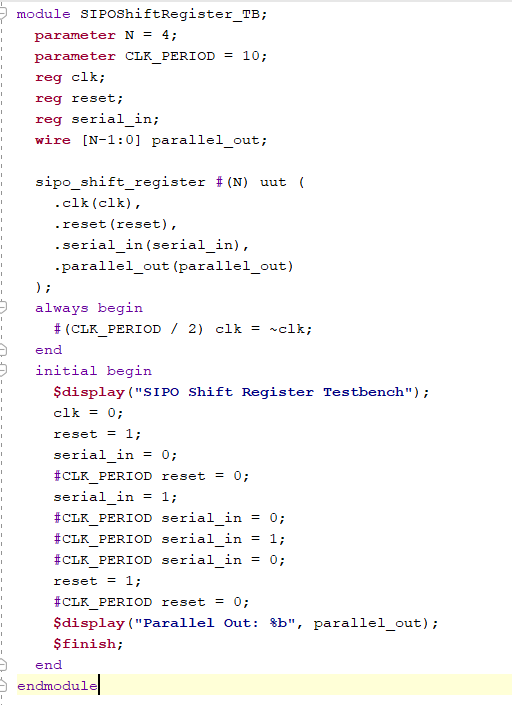


1. **Serial In Parallel Out Shift Register :-**

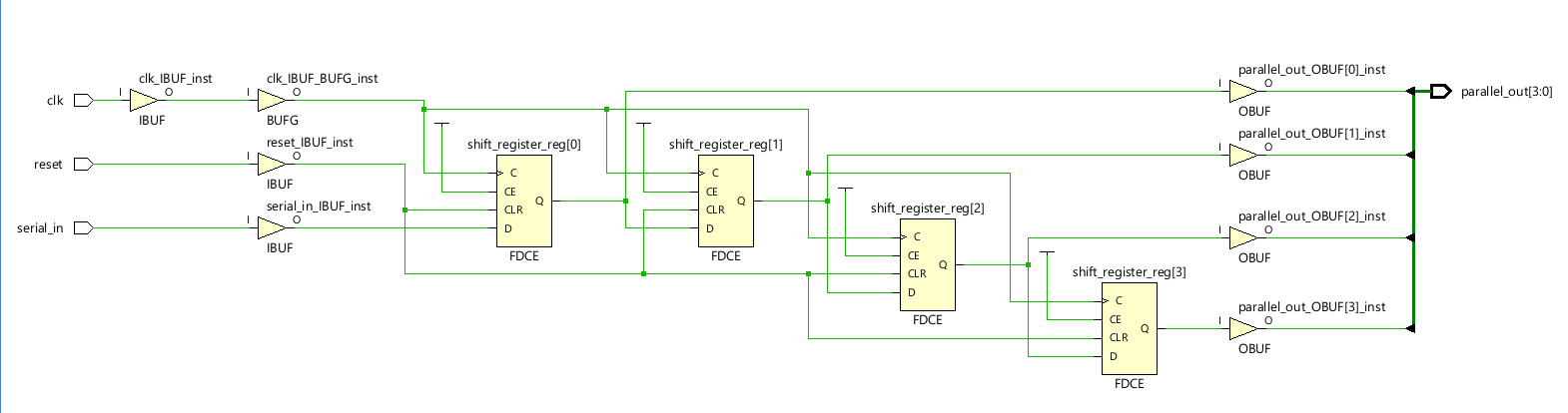
Verilog Code:



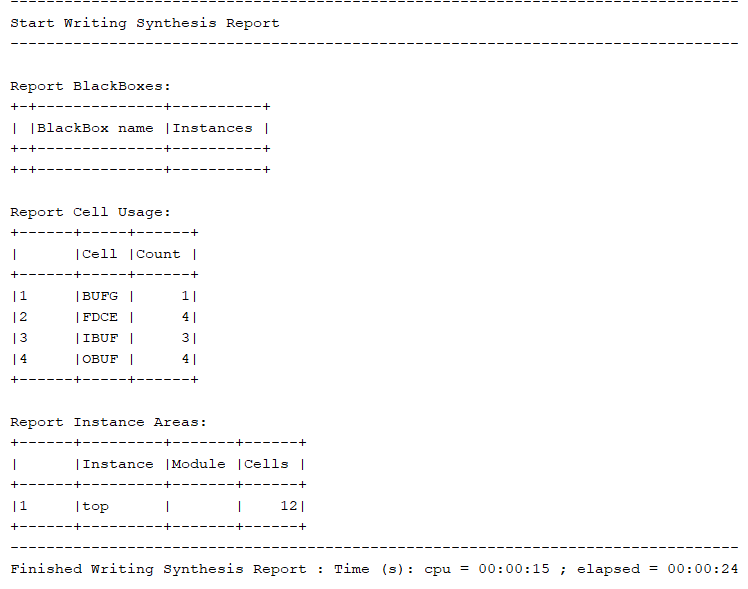
Test Bench:



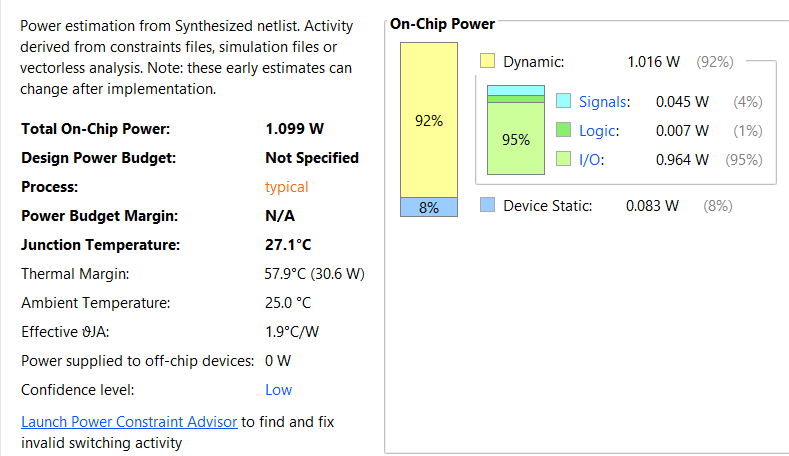
RTL Schematic:



Synthesis Report:

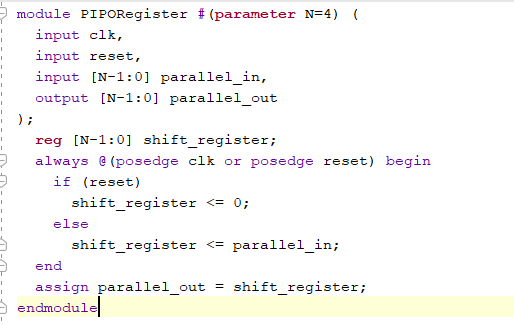


Power Report:

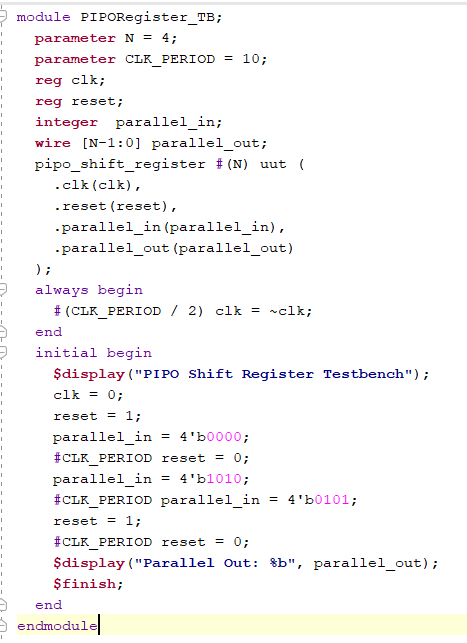


1. **Parallel In Parallel Out Register :-**

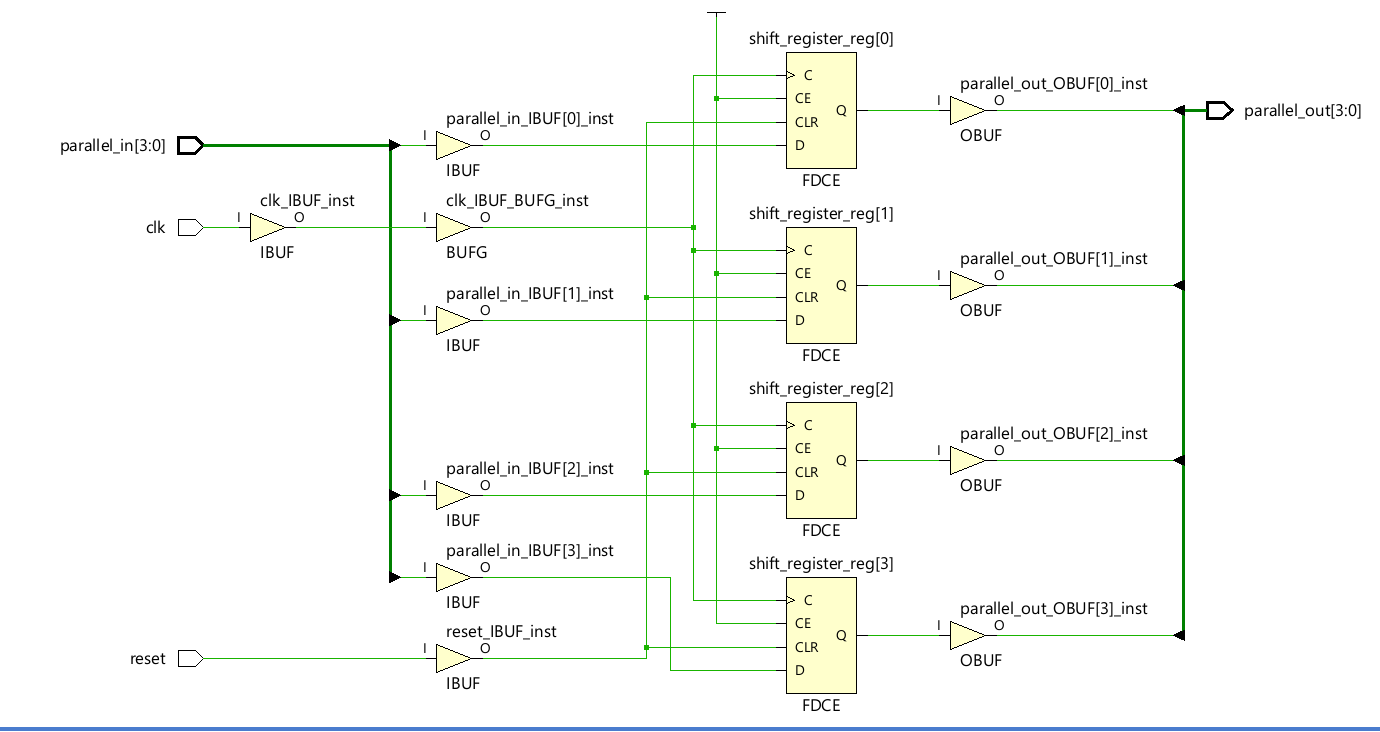
Verilog Code:



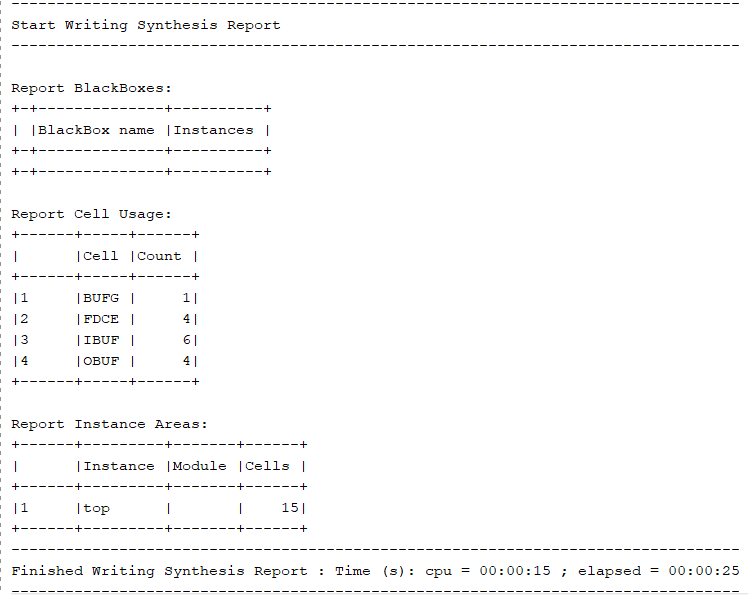
Test Bench:



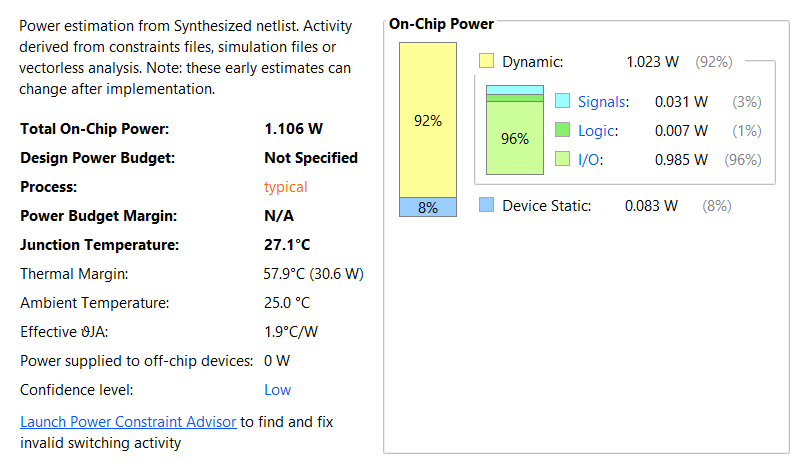
RTL Schematic:



Synthesis Report:

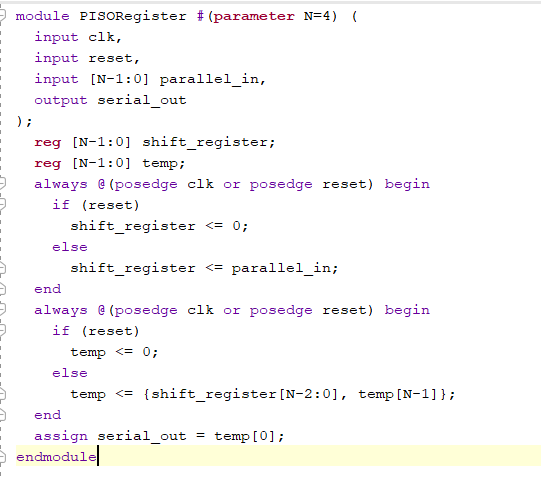


Power Report:

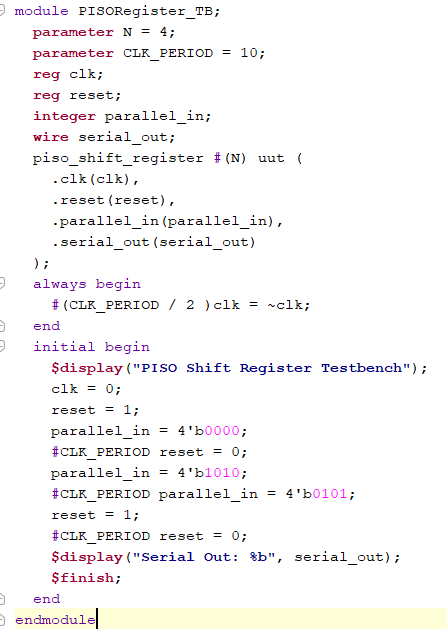


1. **Parallel In Serial Out Register :-**

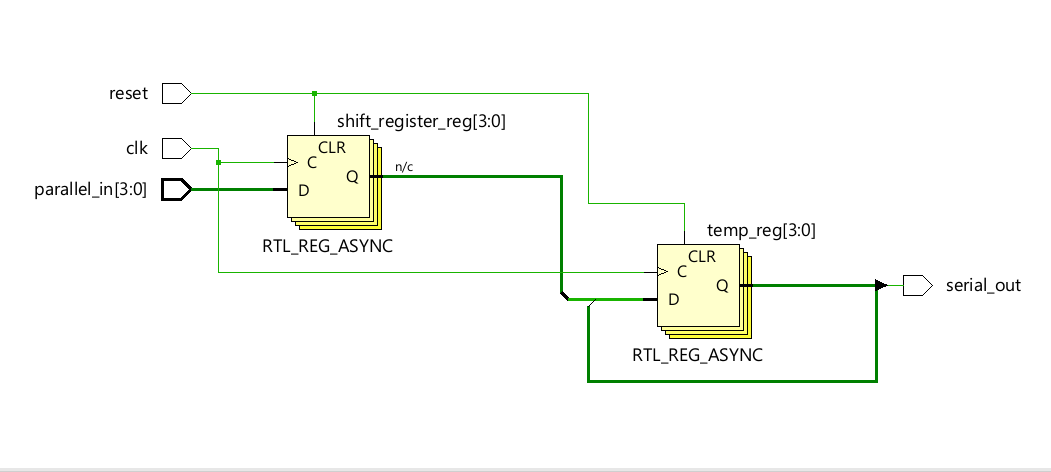
Verilog Code:



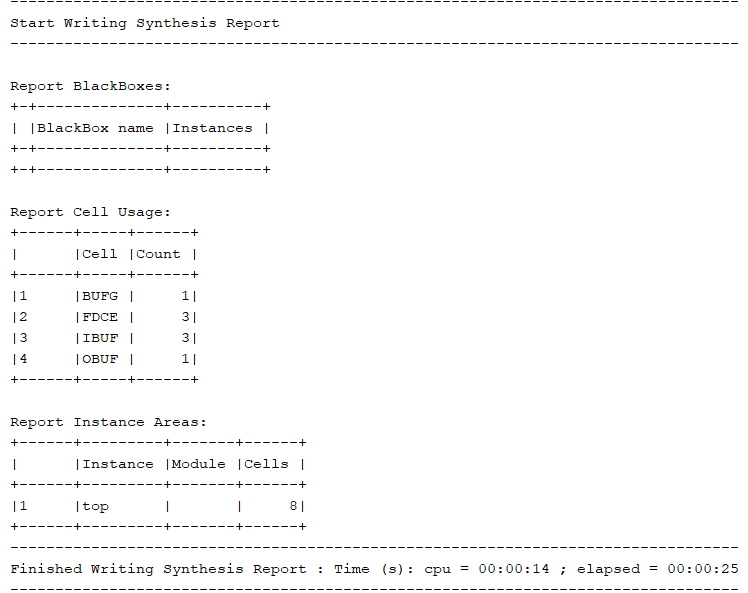
Test Bench:



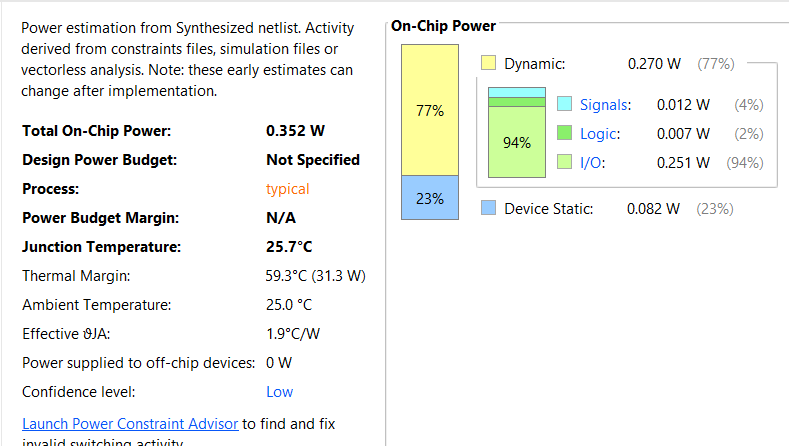
RTL Schematic:



Synthesis Report:

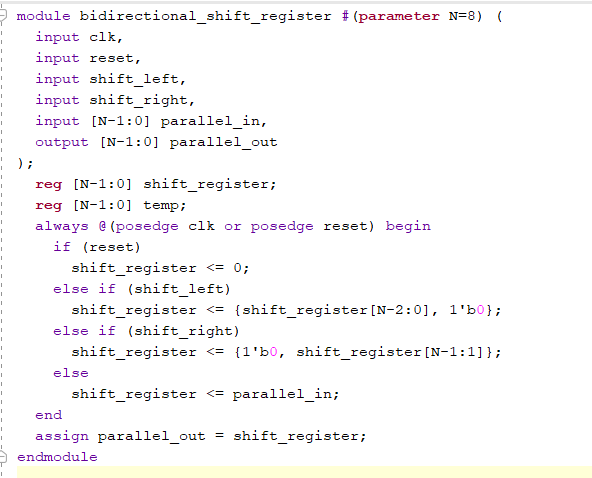


Power Report:

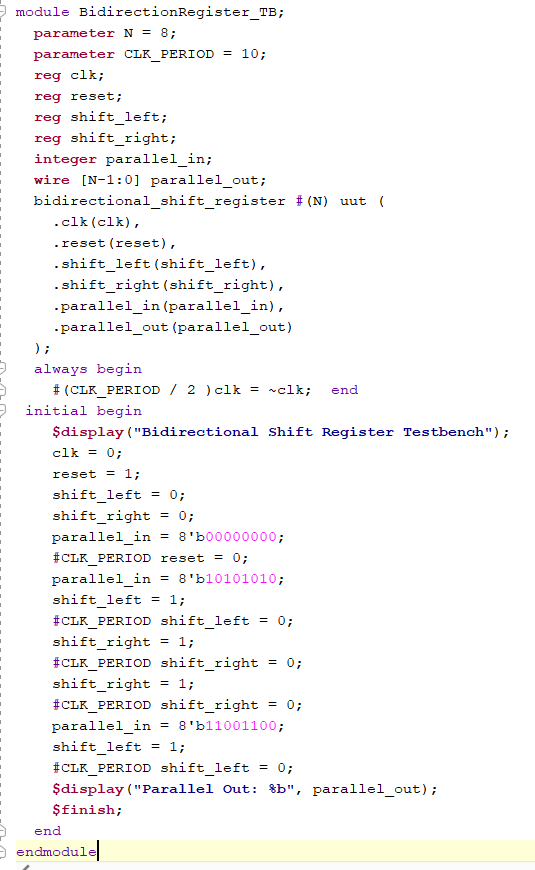


1. **Bi-Direction Shift Register :-**

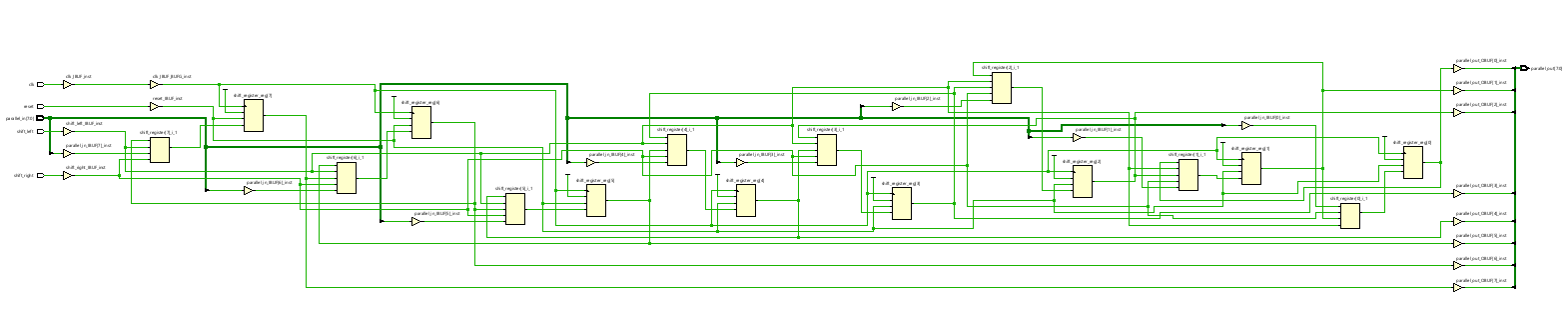
Verilog Code:



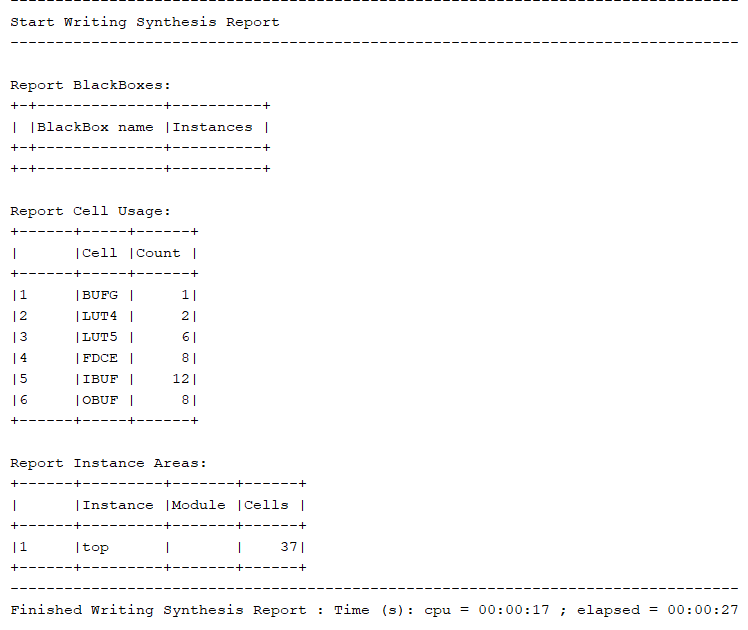
Test Bench:



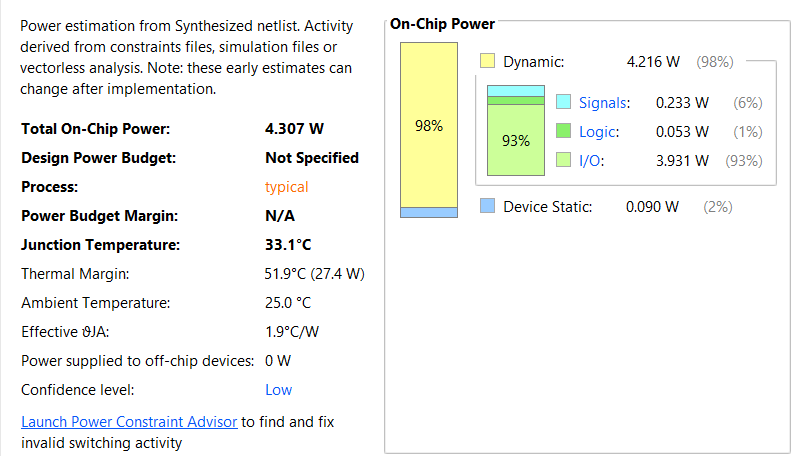
RTL Schematic:



Synthesis Report:

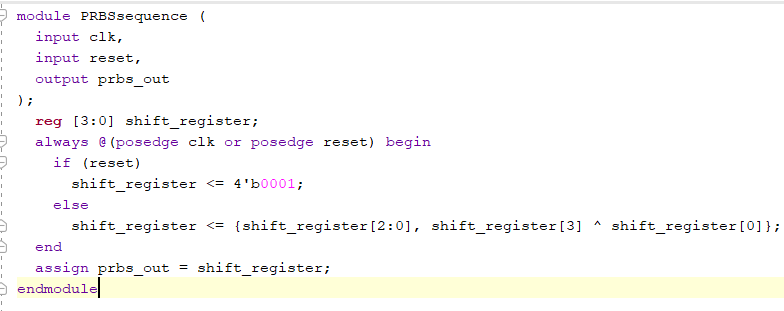


Power Report:

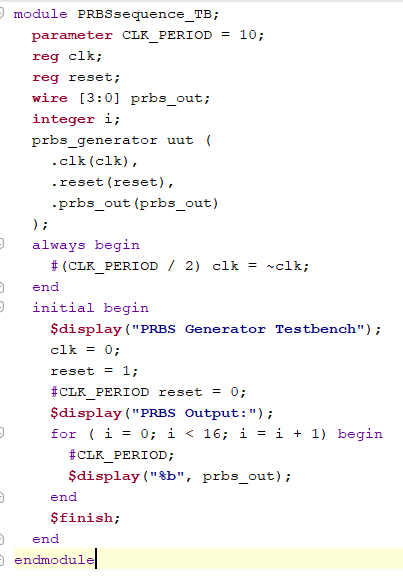


1. **PRBS Sequence Generator :-**

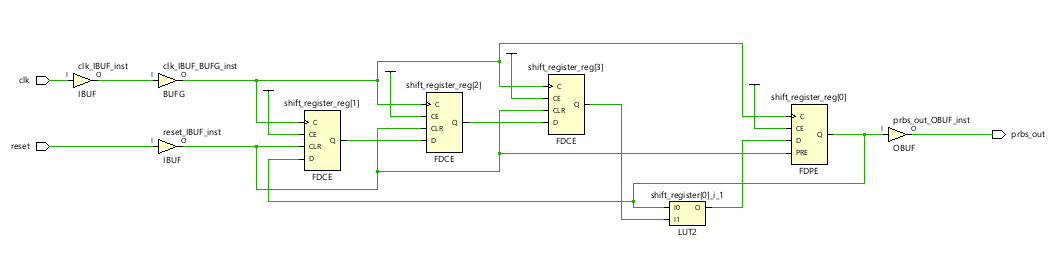
Verilog Code:



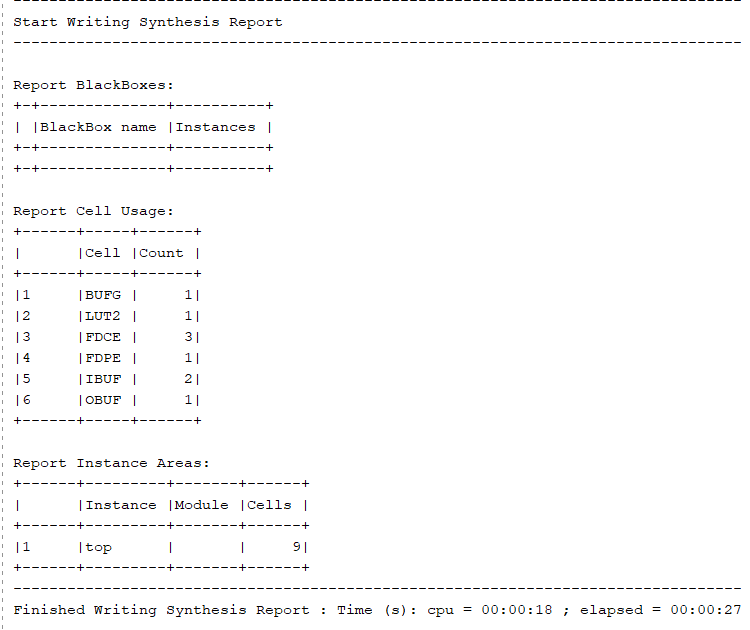
Test Bench:



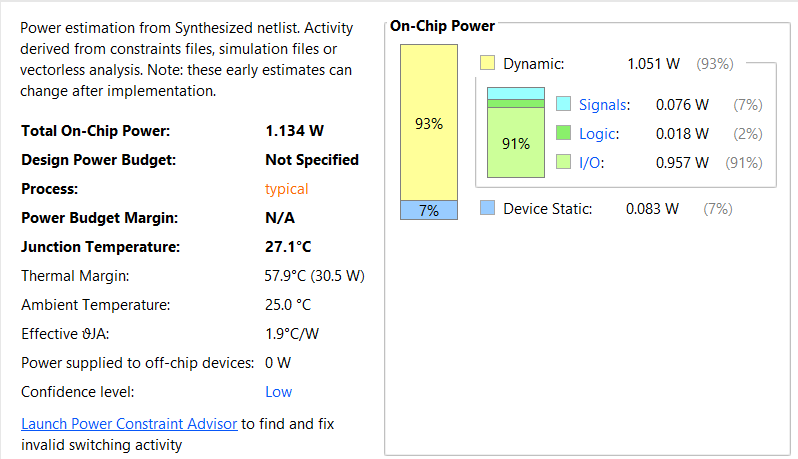
RTL Schematic:



Synthesis Report:

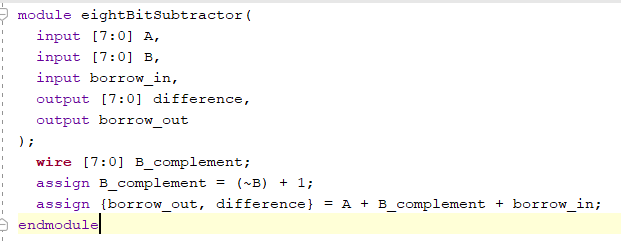


Power Report:

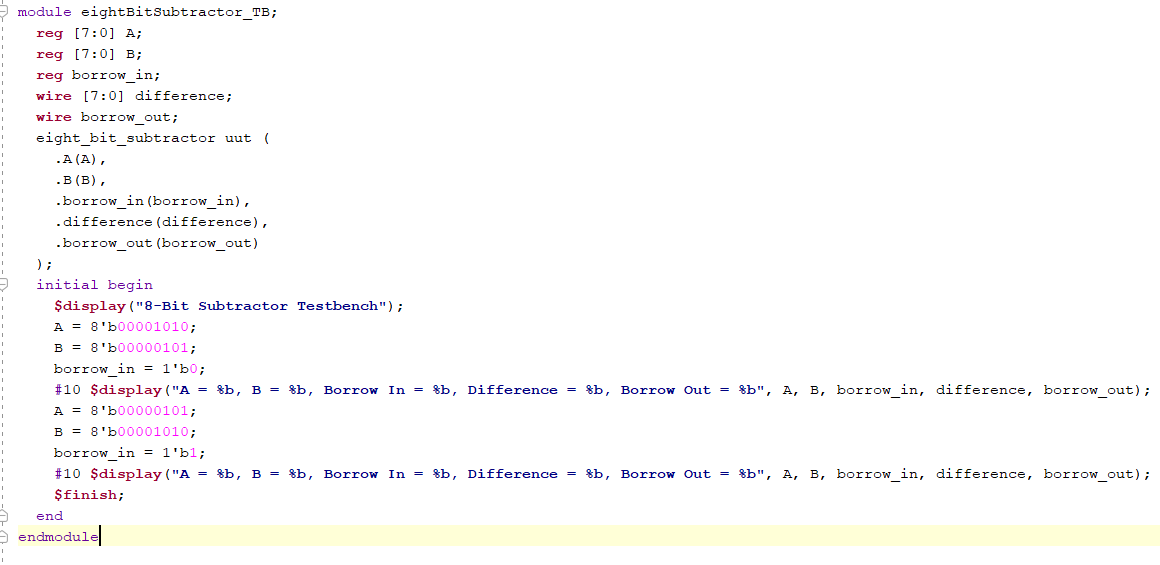


1. **8-Bit Subtractor :-**

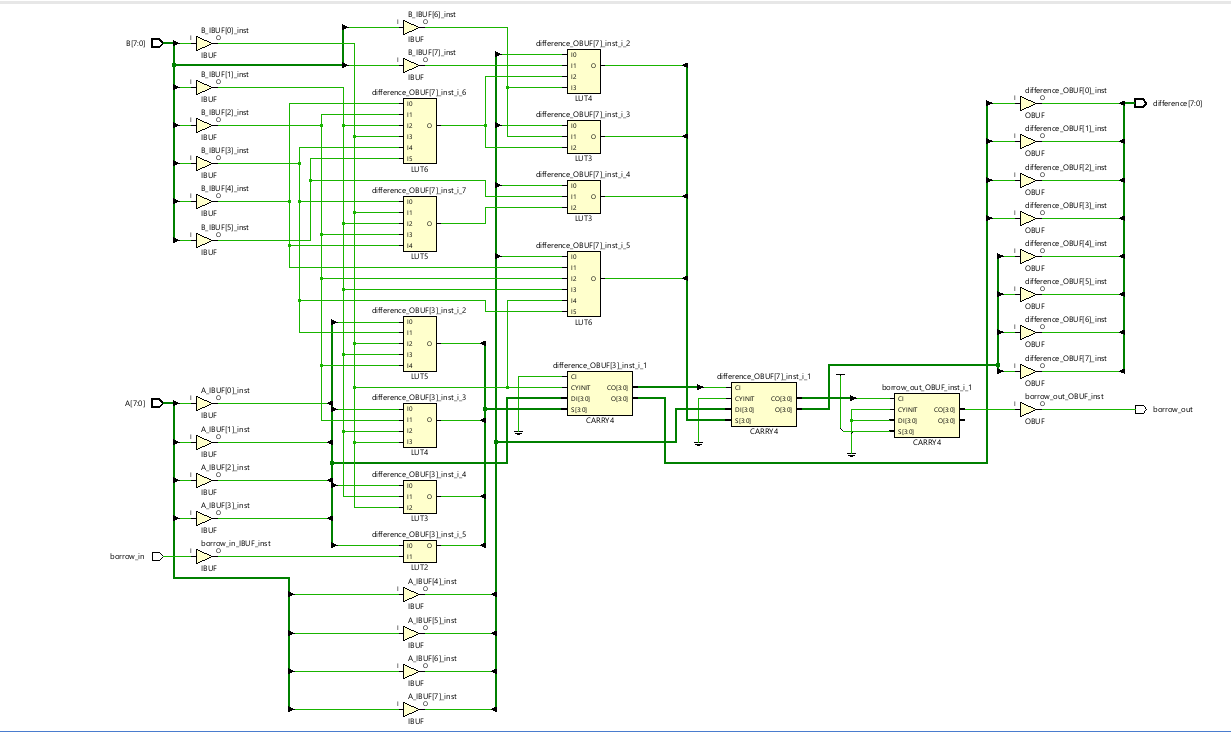
Verilog Code:



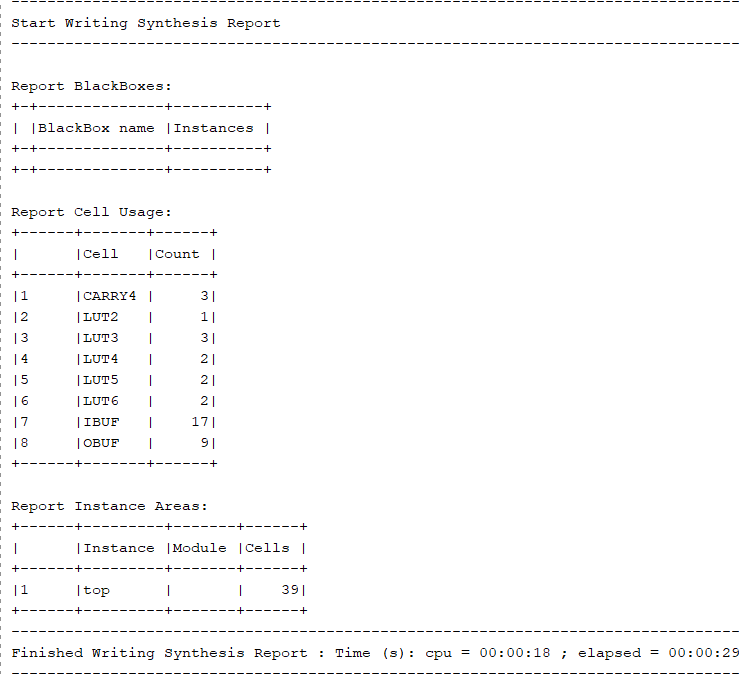
Test Bench:



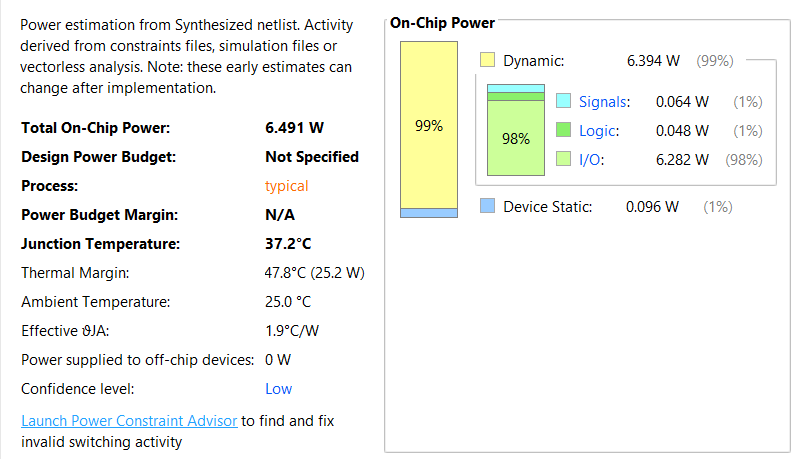
RTL Schematic:



Synthesis Report:

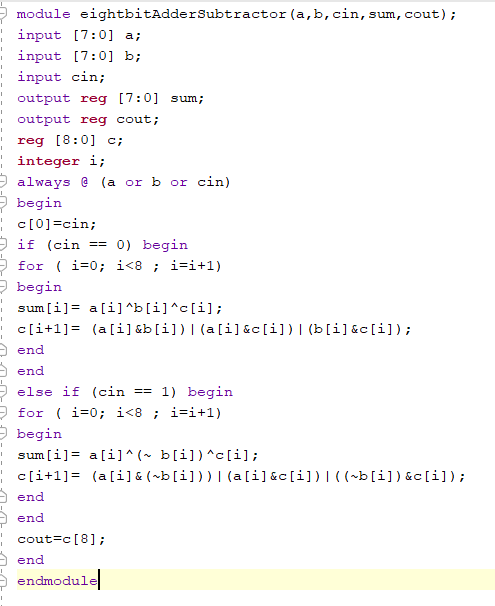


Power Report:

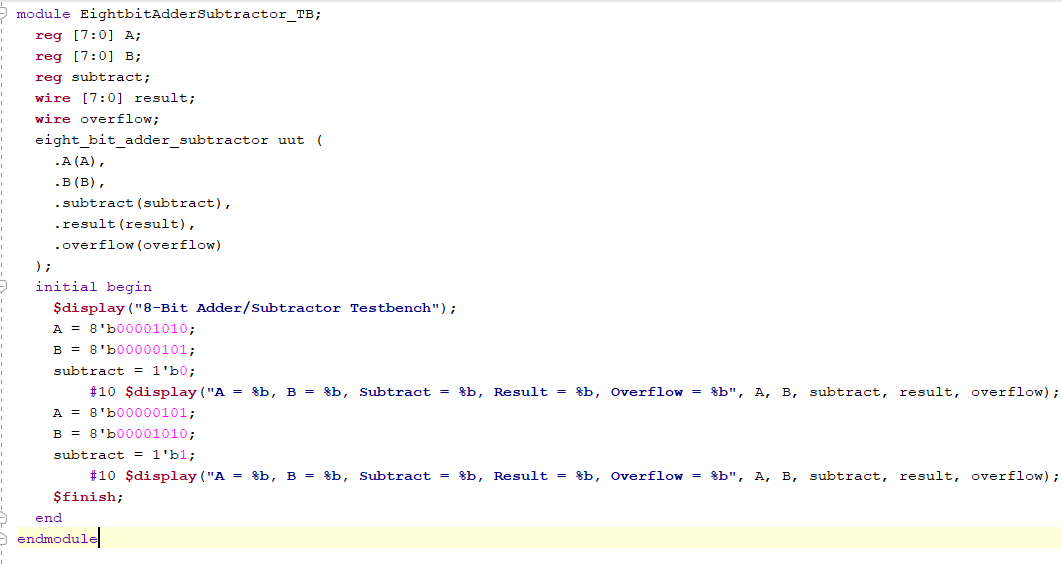


1. **8-Bit Adder/Subtractor :-**

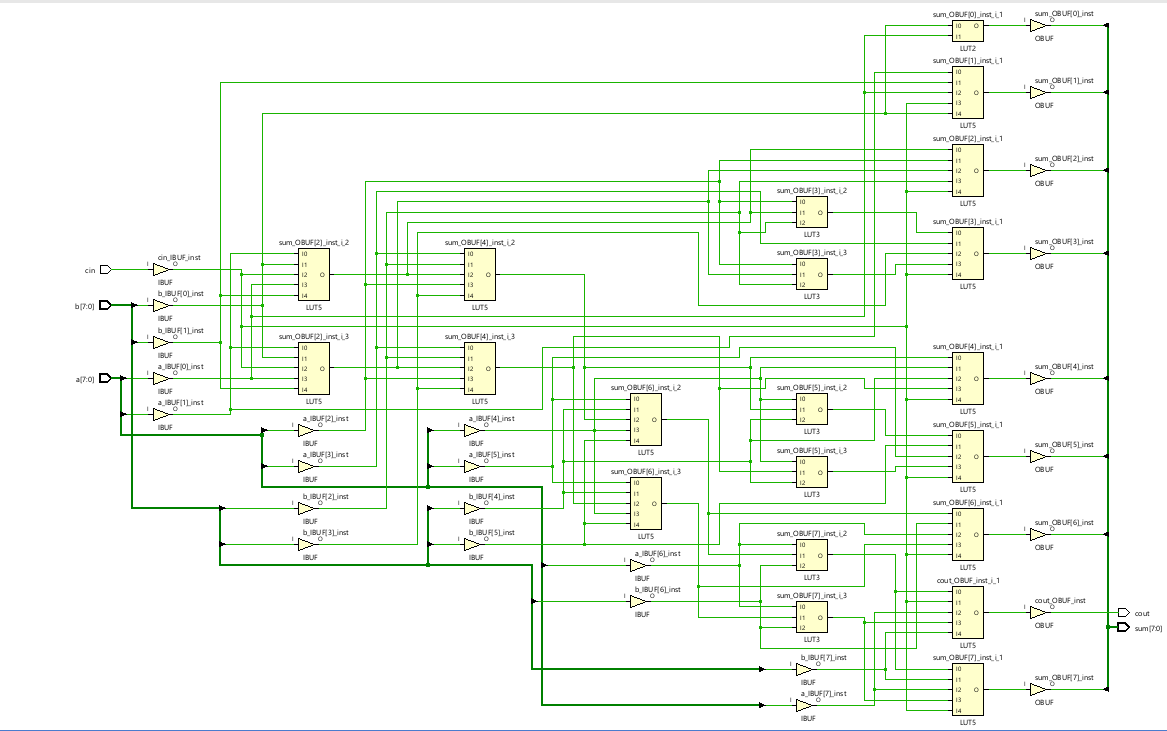
Verilog Code:



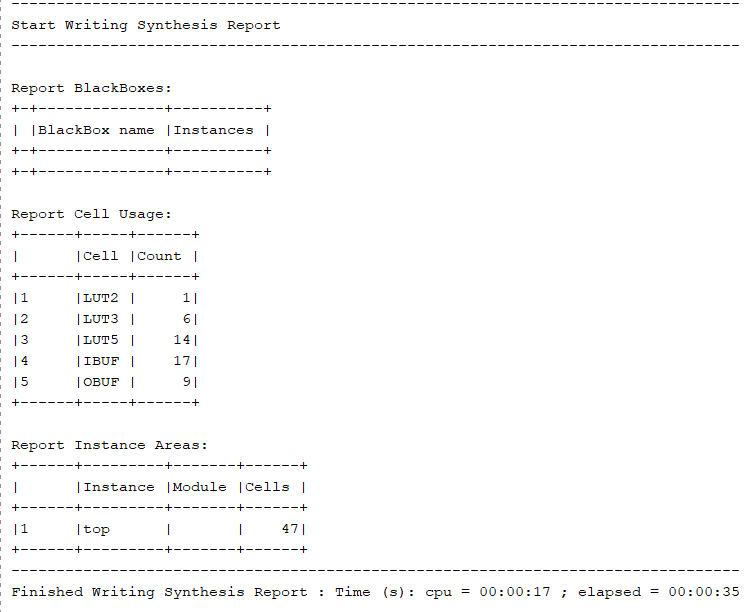
Test Bench:



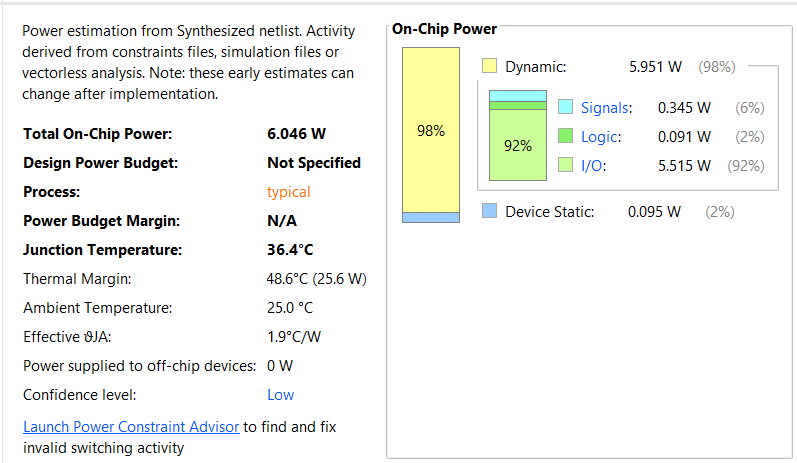
RTL Schematic:



Synthesis Report:

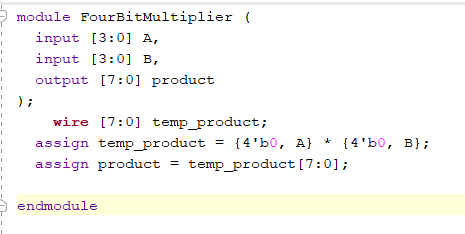


Power report:

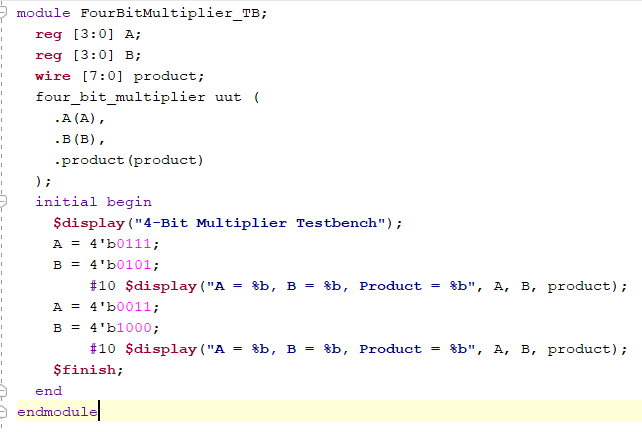


1. **4-Bit Multiplier :-**

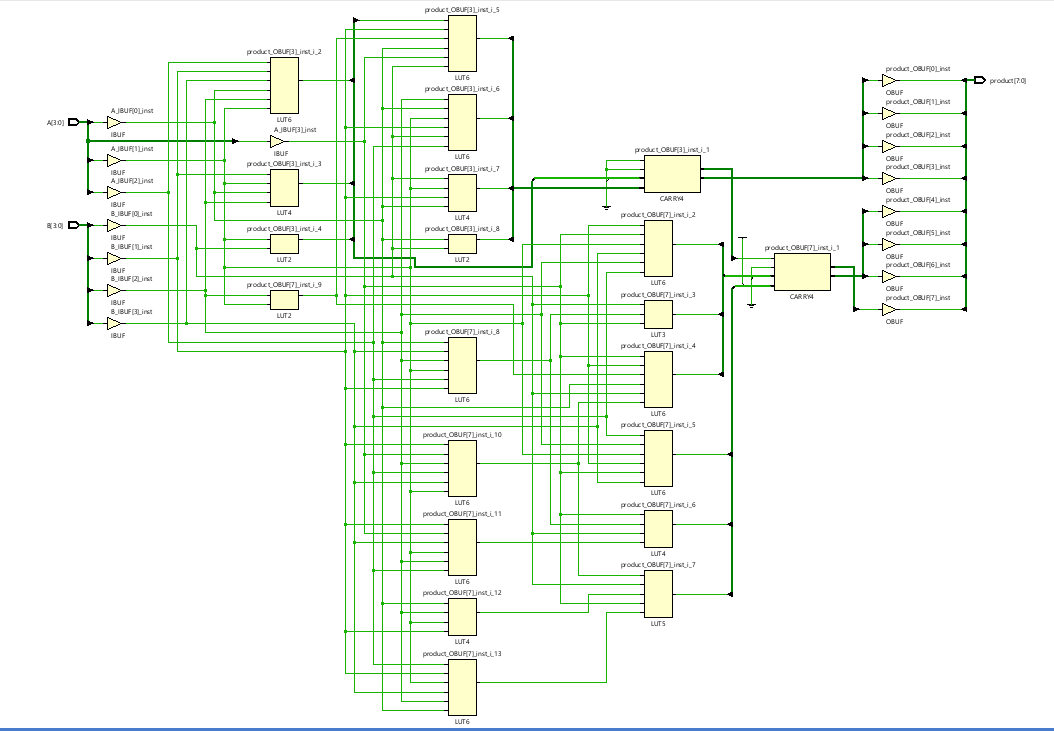
Verilog Code:



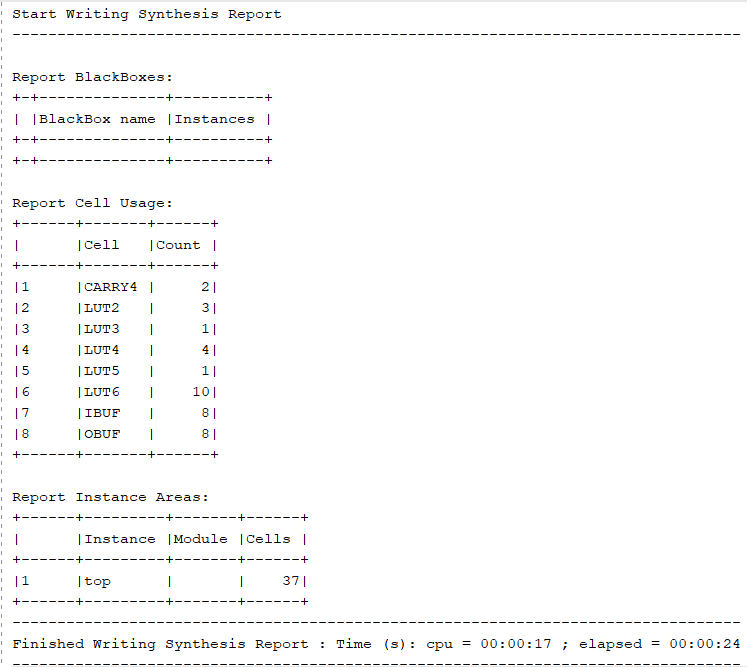
Test Bench:



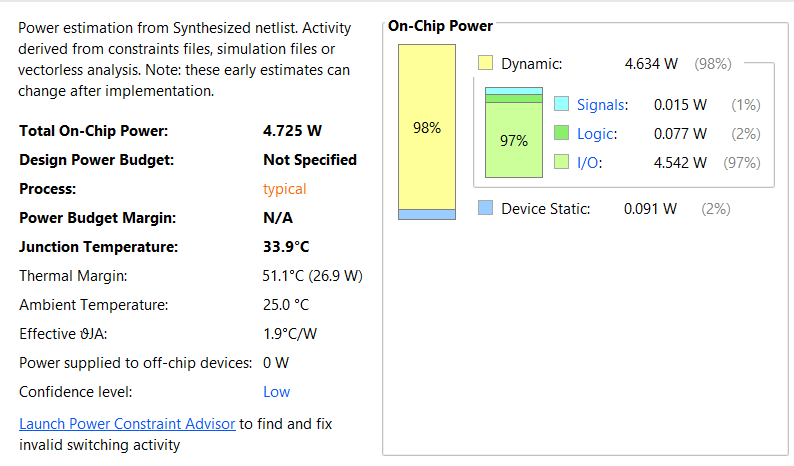
RTL Schematic:



Synthesis Report:

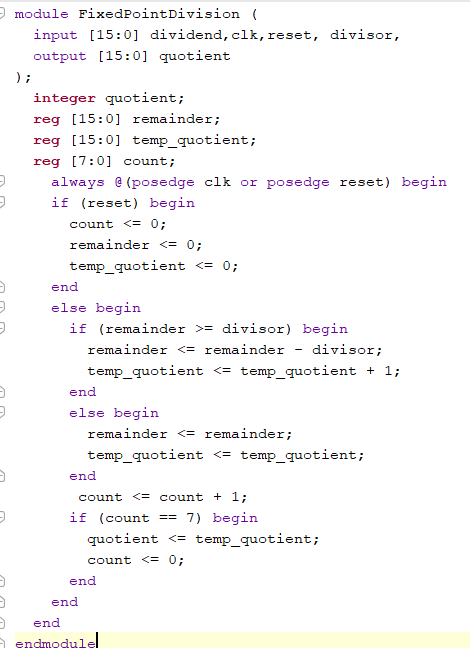


Power Report:

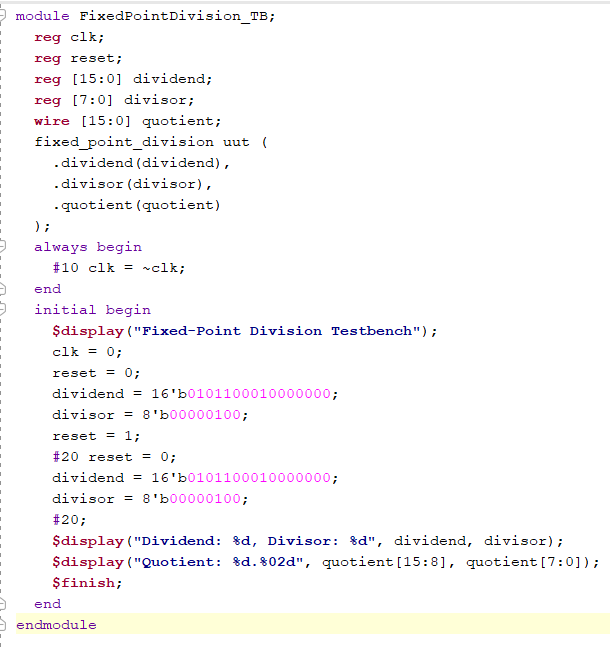


1. **Fixed Point Division :-**

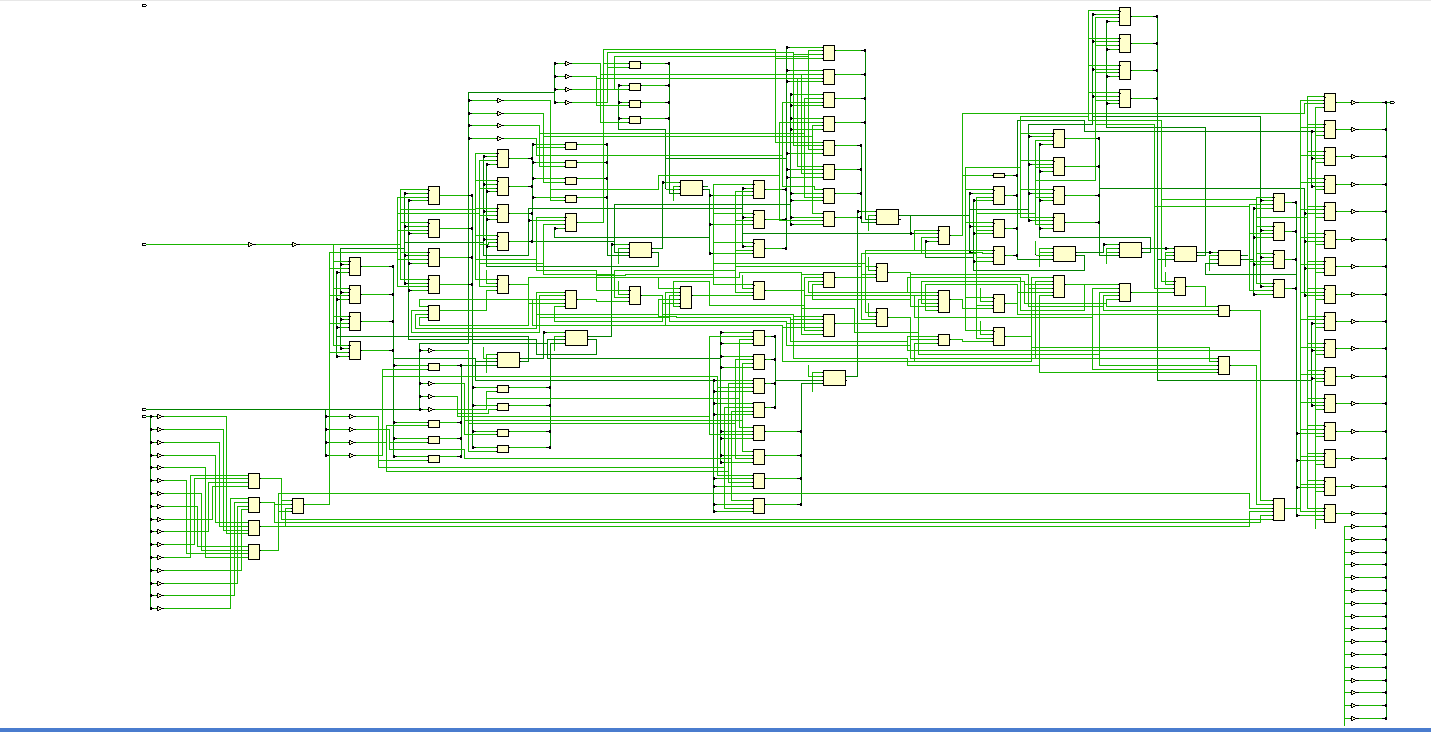
Verilog Code:



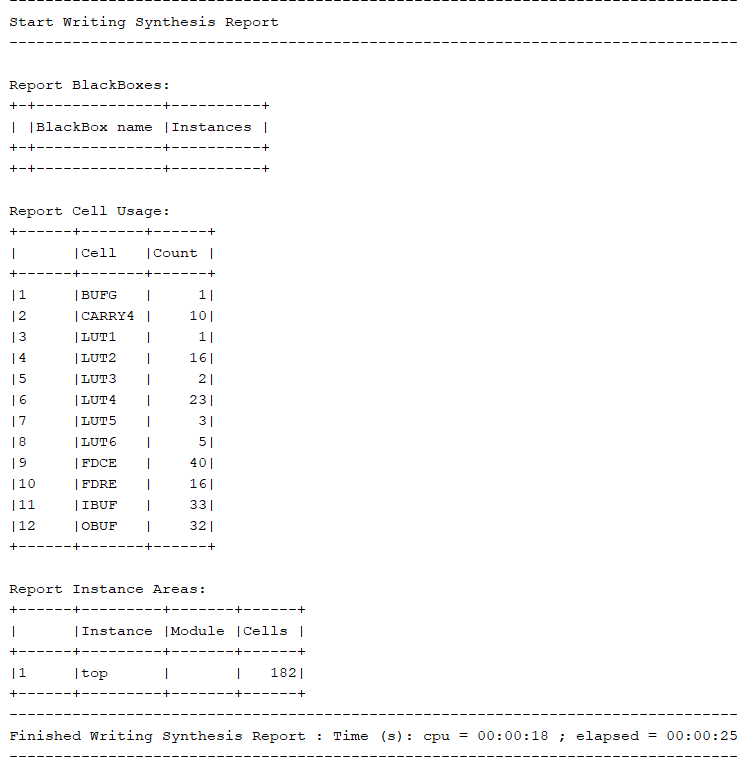
Test Bench:



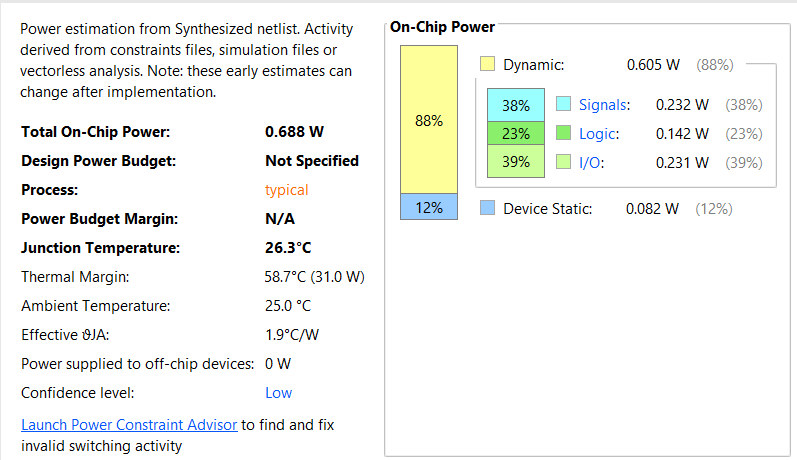
RTL Schematic:



Synthesis Report:

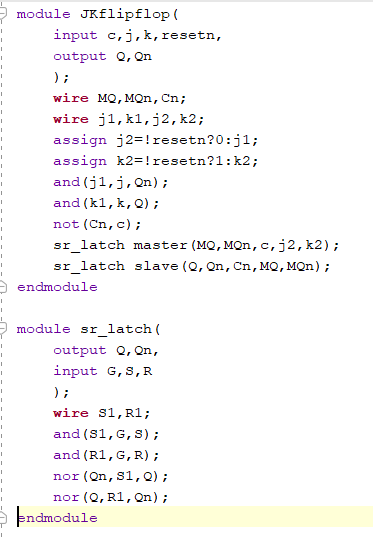


Power Report:

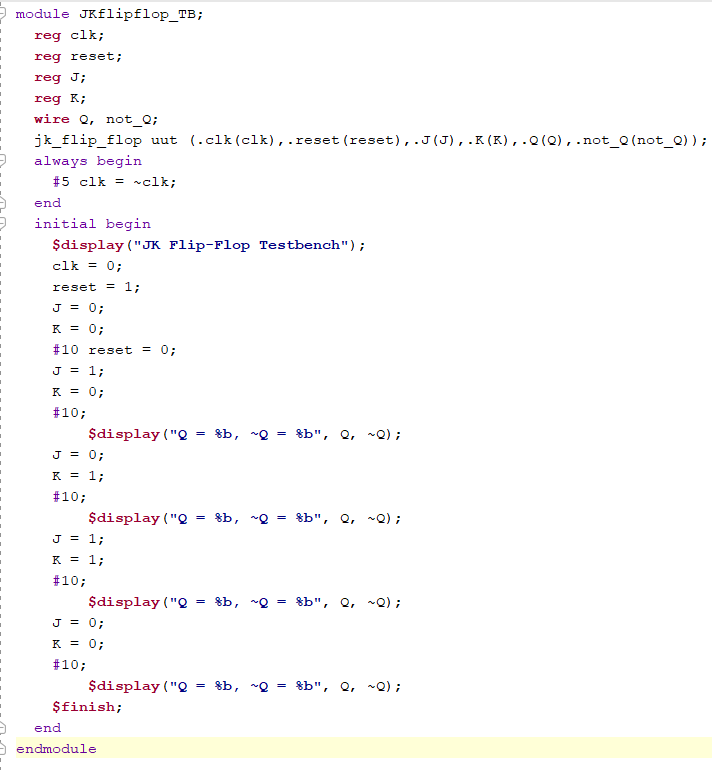


1. **Master Slave JK Flip Flop :-**

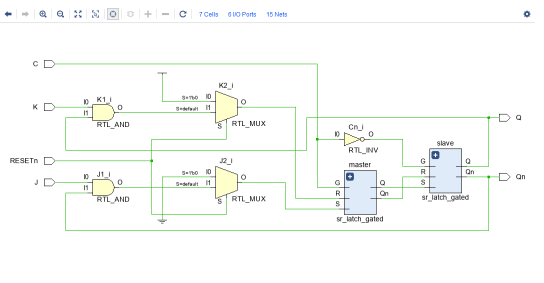
Verilog Code:



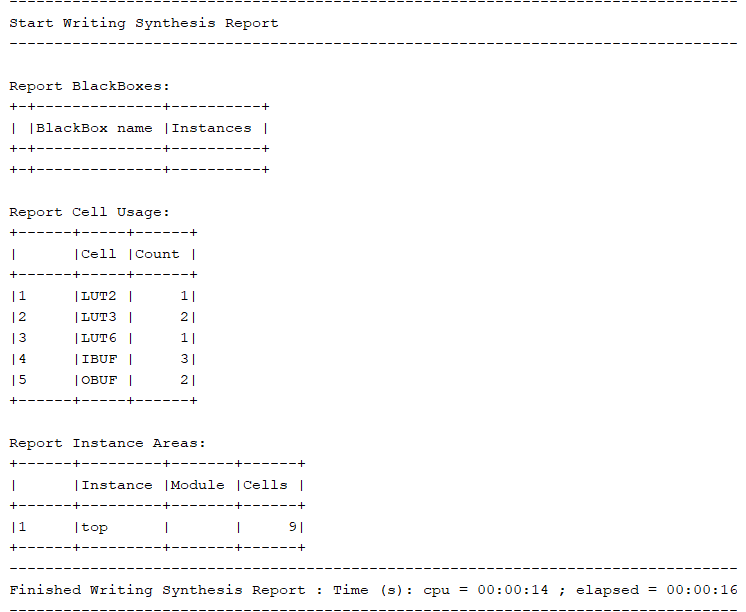
Test Bench:



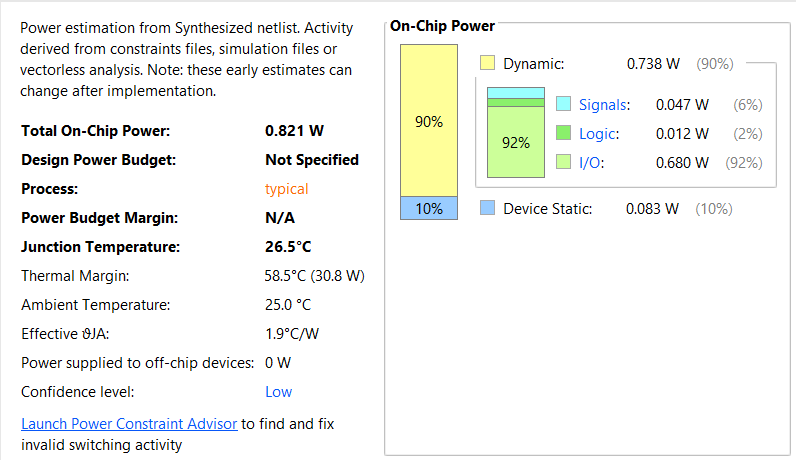
RTL Schematic:



Synthesis Report:

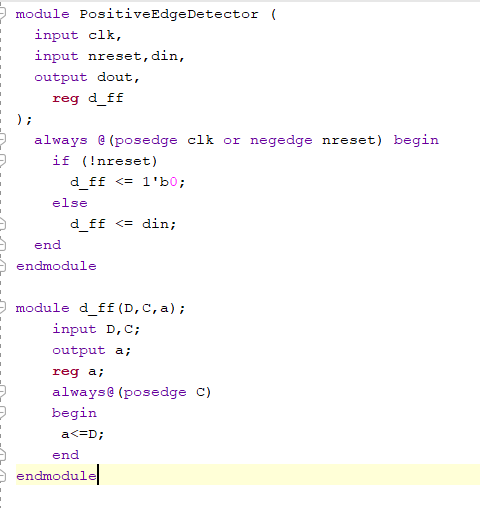


Power Report:

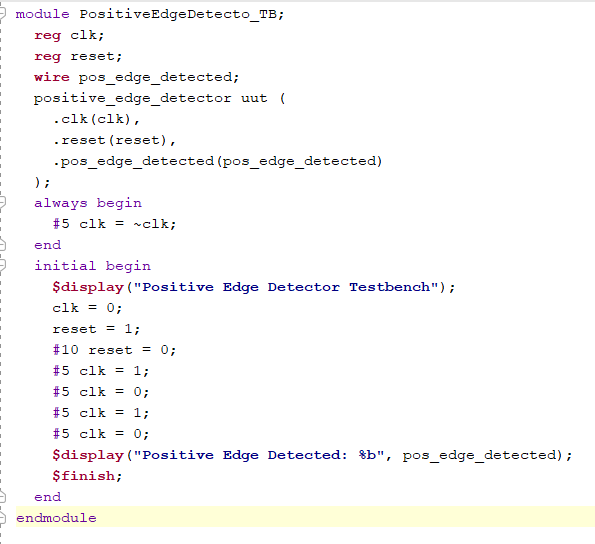


1. **Positive Edge Detector :-**

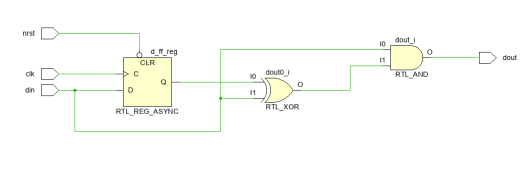
Verilog Code:



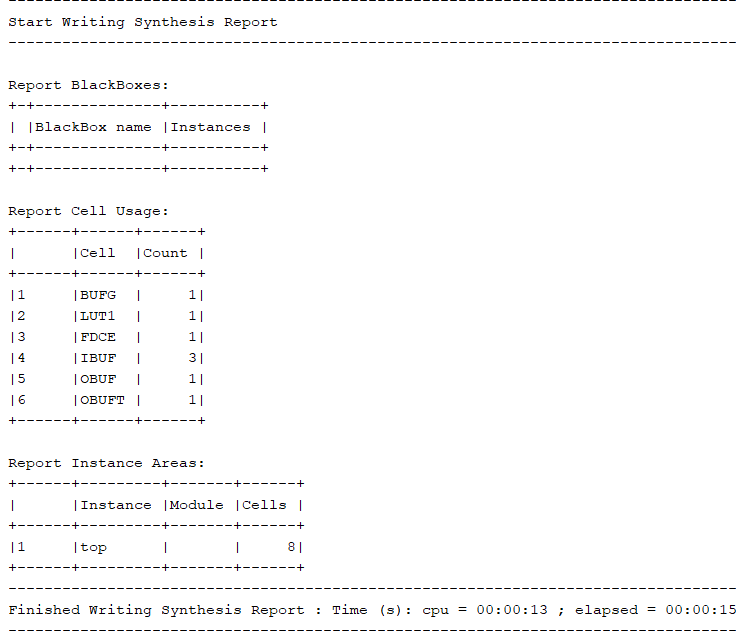
Test Bench:



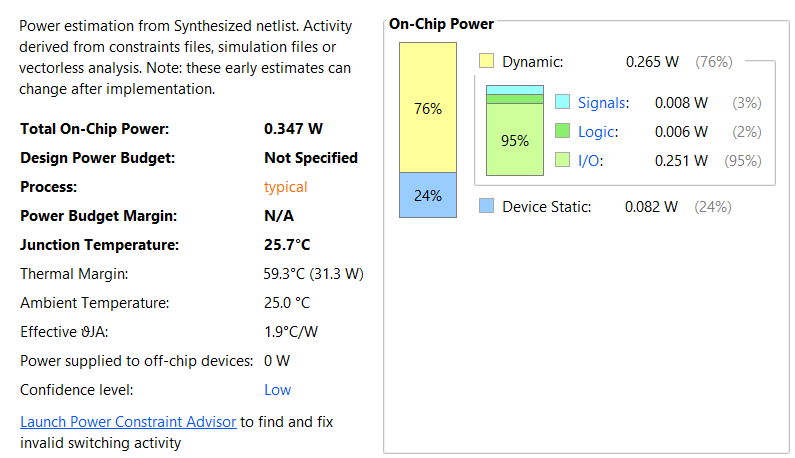
RTL Schematic:



Synthesis Report:

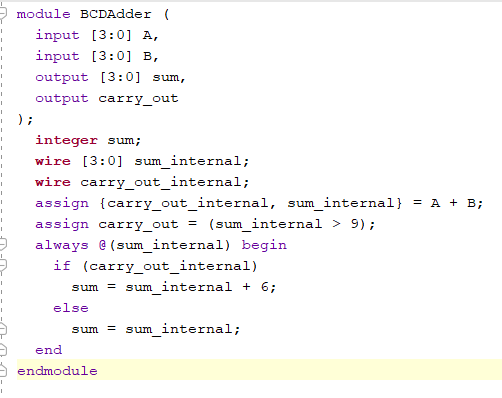


Power Report:

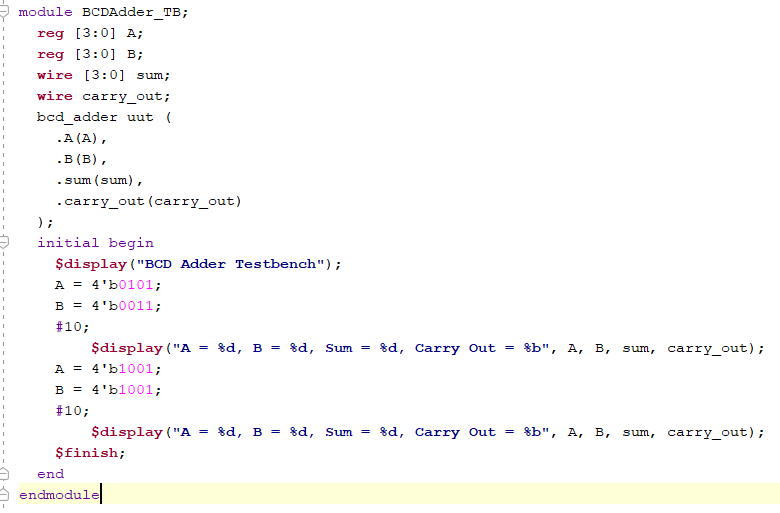


1. **BCD Adder :-**

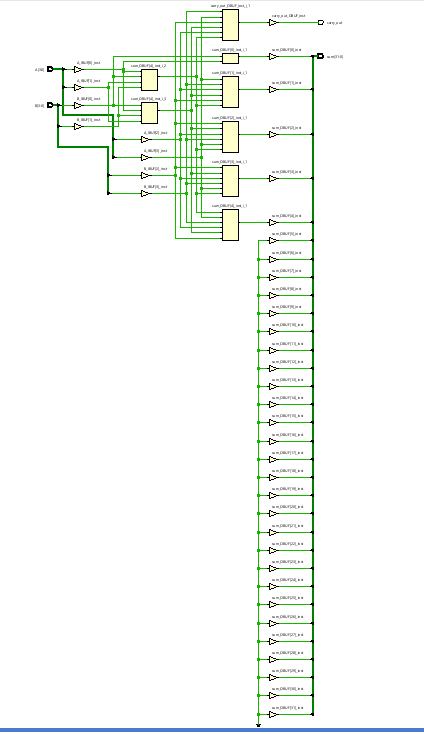
Verilog Code:



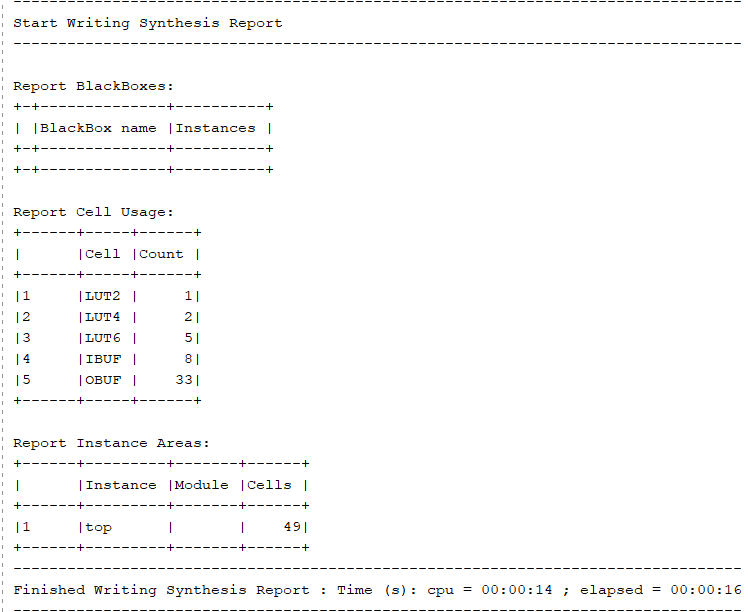
Test Bench:



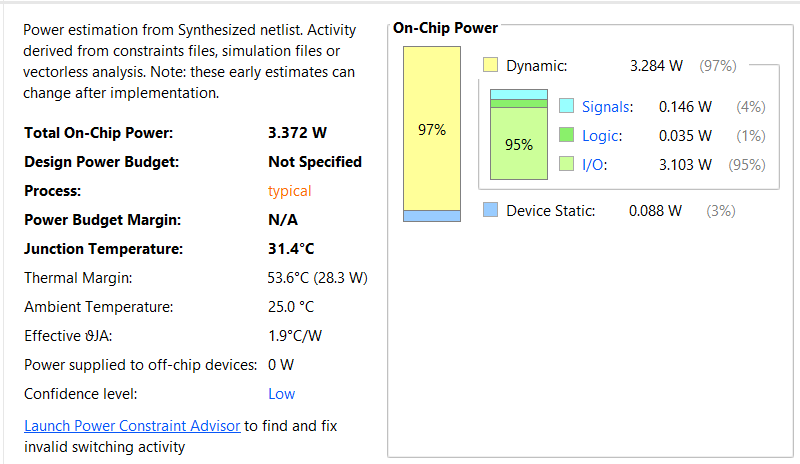
RTL Schematic:



Synthesis Report;

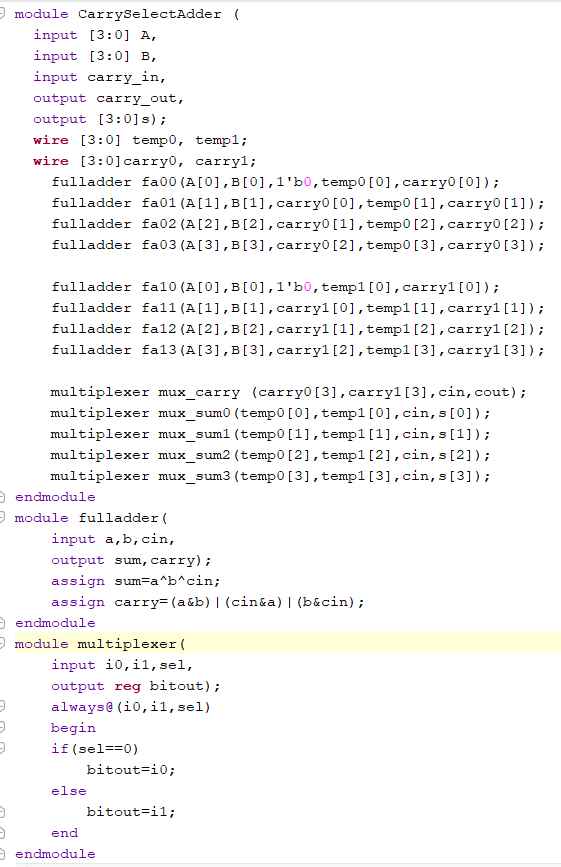


Power Report:

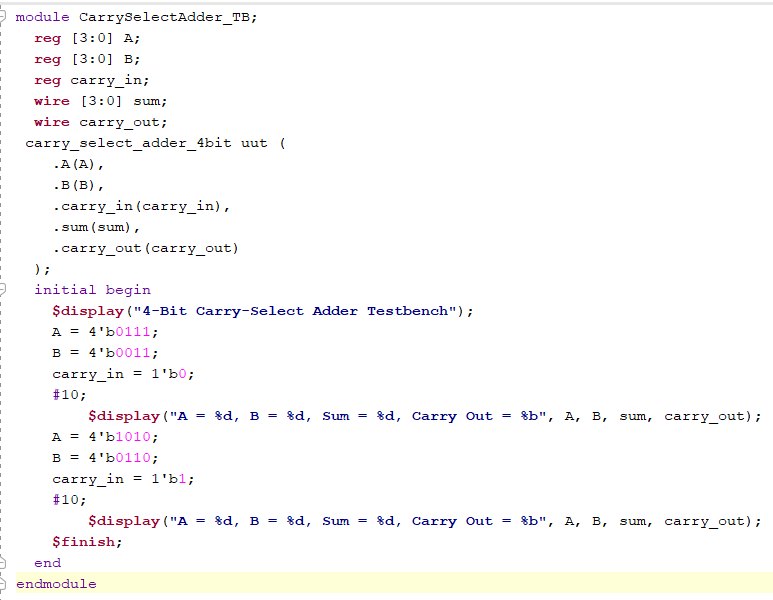


1. **4-Bit Carry Select Adder :-**

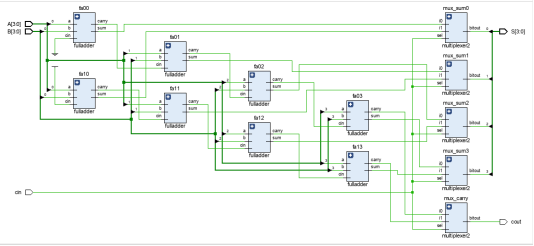
Verilog Code:



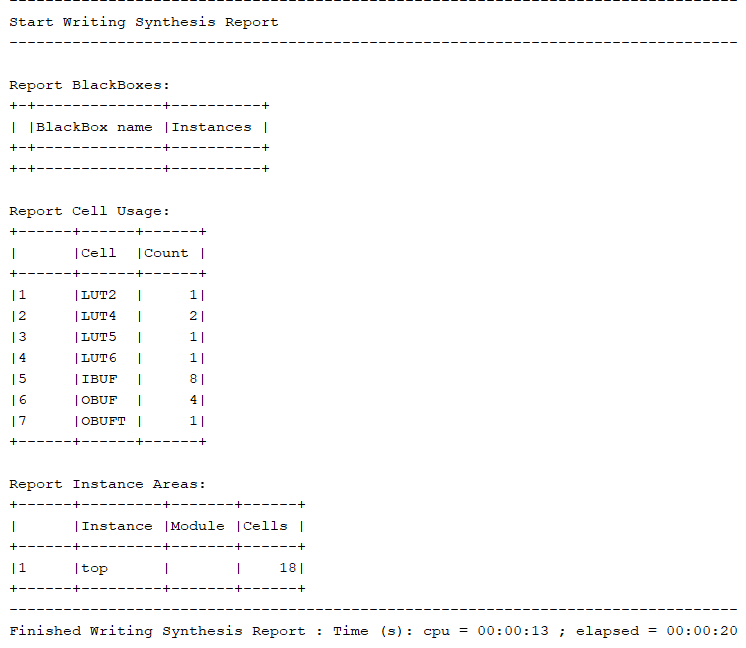
Test Bench:



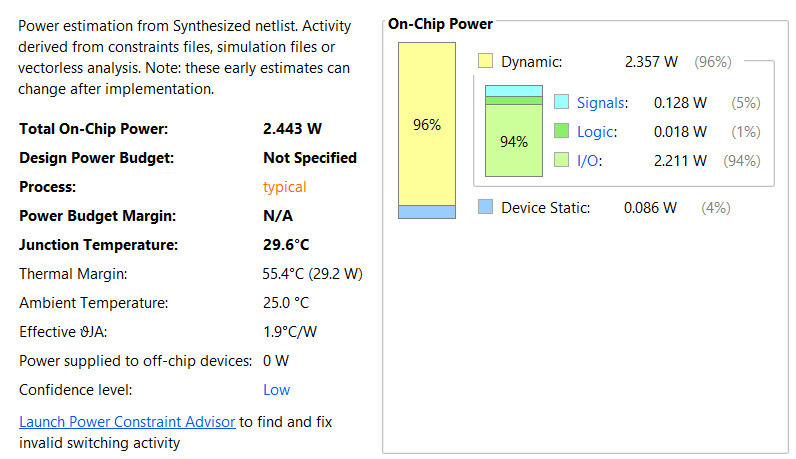
RTL Schematic:



Synthesis Report:

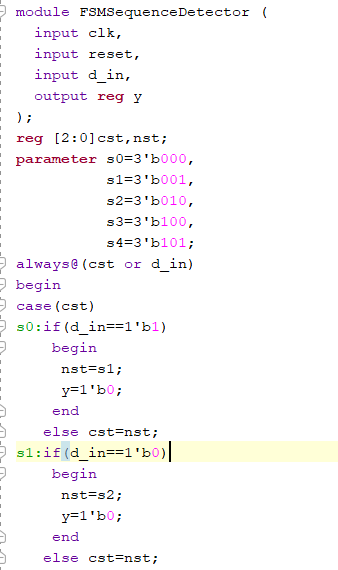


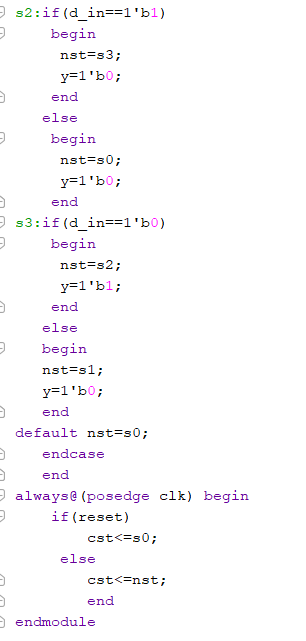
Power Report:



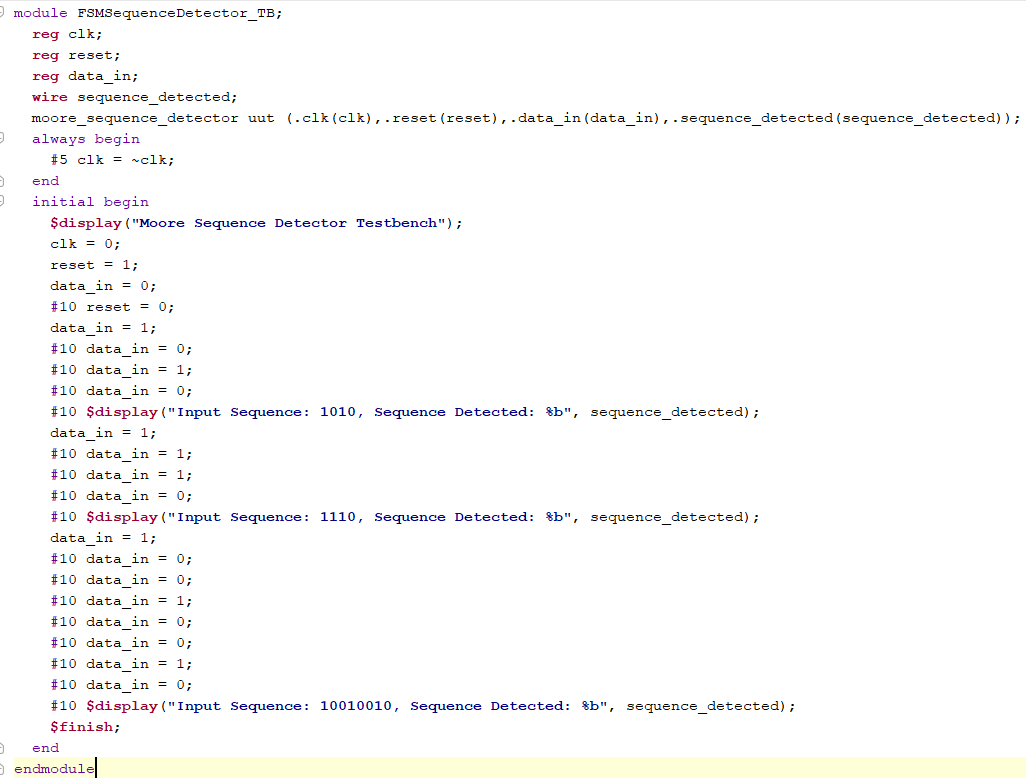
1. **Moore FSM 1010 Sequence Detector :-**

Verilog Code:

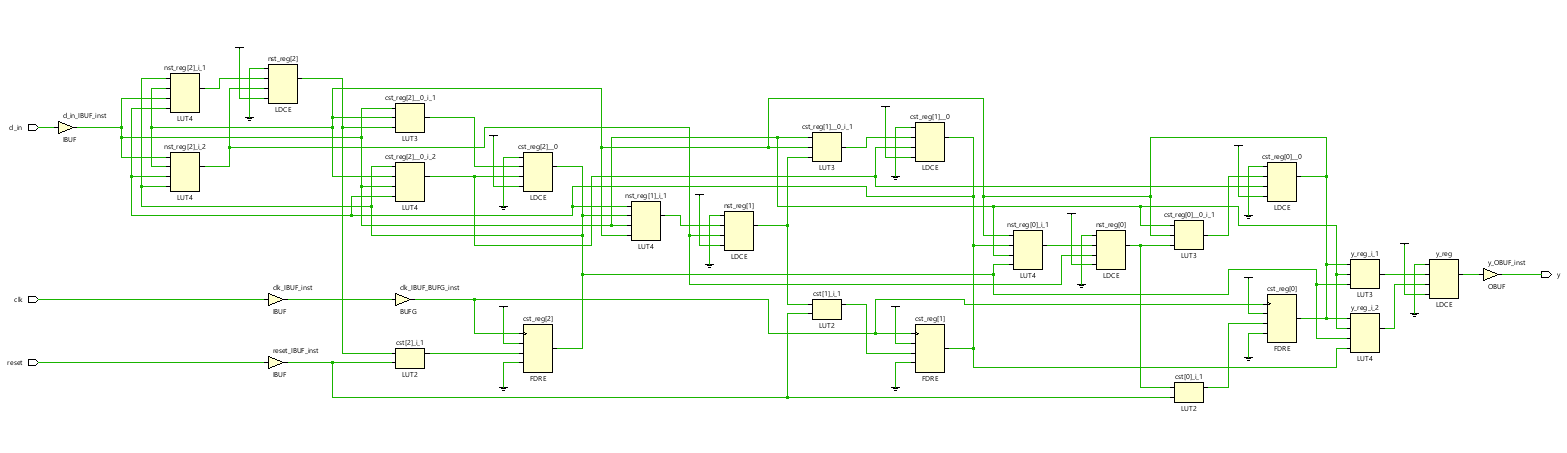




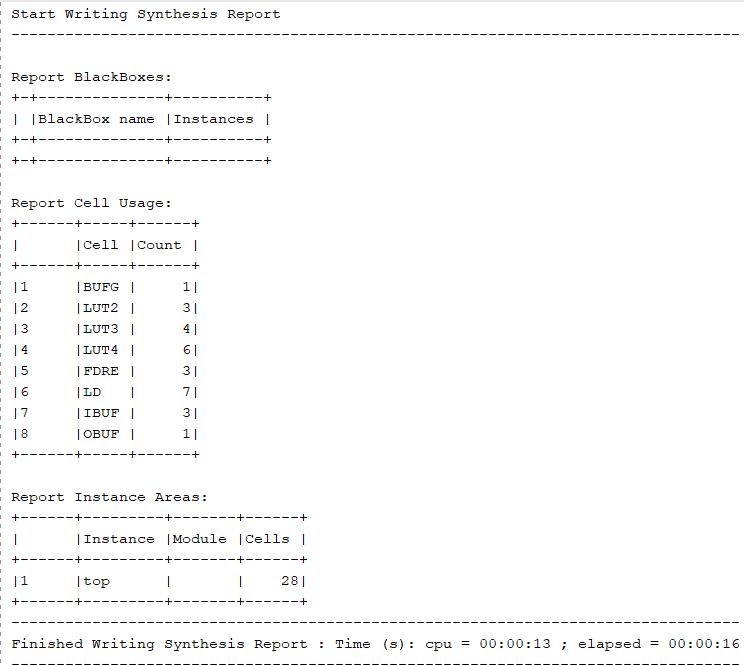
Test Bench:



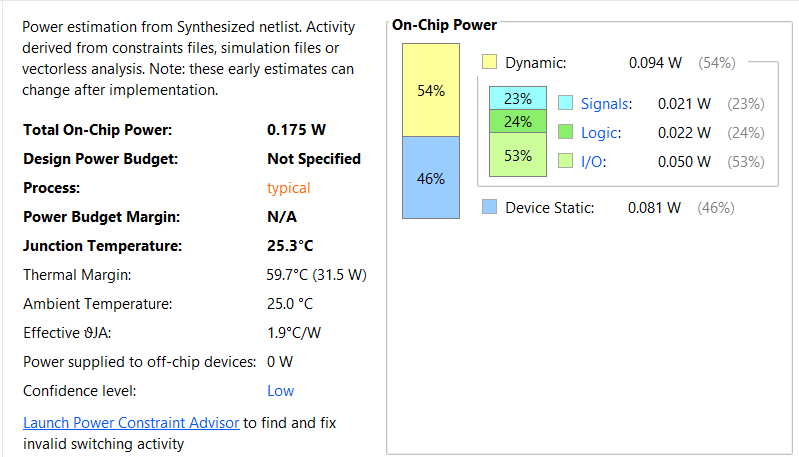
RTL Schematic:



Synthesis Report:

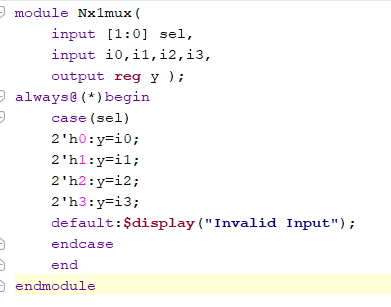


Power Report:

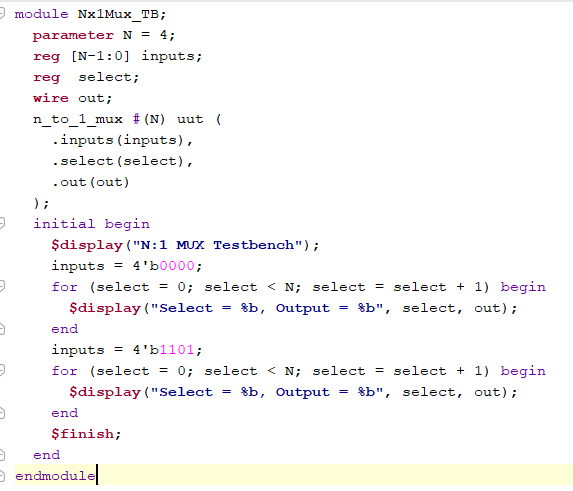


1. **N:1 Mux :-**

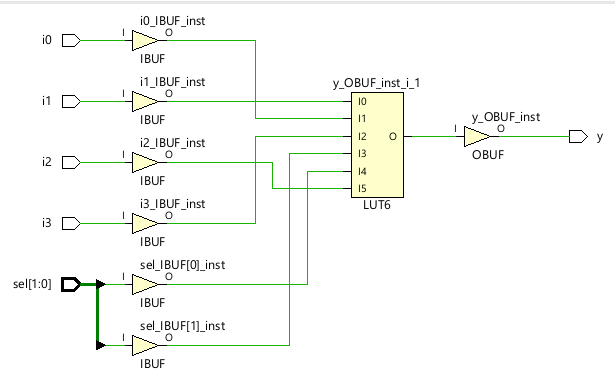
Verilog Code:



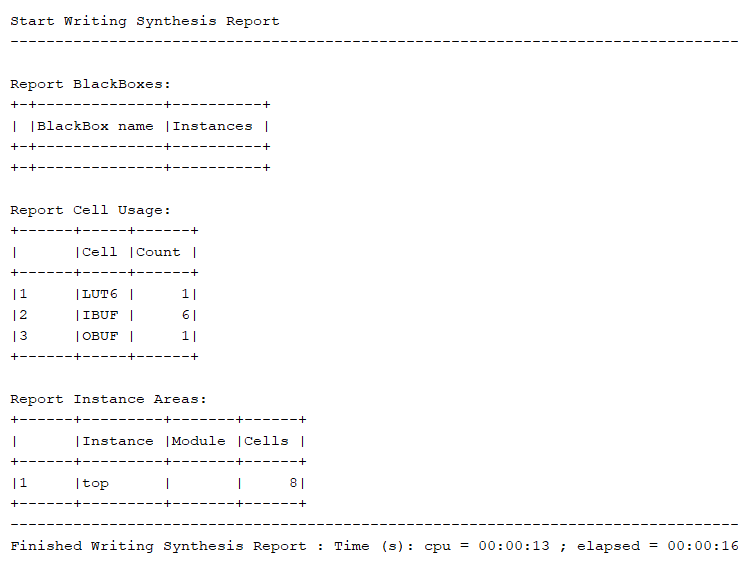
Test Bench:



RTL Schematic:



Synthesis Report:



Power Report:

